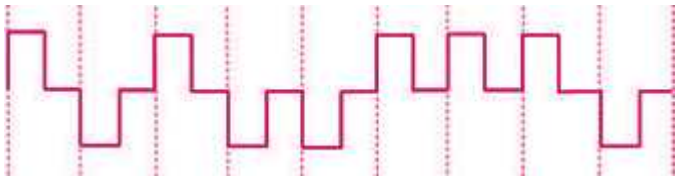


Digital Communication

LABORATORY MANUAL

ELECTRONICS & COMMUNICATION ENGINEERING

COLLEGE OF ENGINEERING AND MANAGEMENT, KOLAGHAT

Revised December 2024

VISION

Pursuing Excellence in Teaching-Learning Process to Produce High Quality Electronics and Communication Engineering Professionals.

MISSION

To enhance the employability of our students by strengthening their creativity with different innovative ideas by imparting high quality technical and professional education with continuous performance improvement monitoring systems.

To carry out research through constant interaction with research organizations and industry.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO-1	Attain a solid foundation in electronics & communication engineering fundamentals with an attitude to pursue continuing education and to succeed in industry/technical profession through global education
PEO-2	Ability to function professionally in an increasingly international and rapidly changing world due to the advances in emerging technologies and concepts.
PEO-3	Exercise excellent leadership qualities on multi-disciplinary and multi-cultural teams at levels appropriate to their experience, which addresses issues in a responsive, ethical and innovative manner.
PEO-4	Contribute to the needs of the society in solving technical problems using electronics & communication engineering principles, tools and practice.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSOs-1	An ability to design and conduct the experiments, analyse and interpret the data using modern software or hard ware tools with proper understanding(basic conceptions) of Electronics and Communication Engineering.
PSOs-2	Ability to identify, formulate & solve problems and apply the knowledge of electronics and communication to develop techno-commercial applications.

COURSE OUTCOMES(Cos)

Course Outcomes of Digital Communication Lab (EC592), Third year 5th Semester, ECE
CO1: Concept of PN Sequence generation using shift register.
CO 2: Analyse the process of converting analog signal to discrete form along with their circuits.
CO3: Analyse various analog to digital techniques along with various line coding methods.
CO4: Concept of different types of ADC converter (Modulation, Demodulation).
CO5: Concept of Different types of Digital Carrier Modulation (Amplitude and Frequency).
CO6: Develop an expression for probability of error of different digital carrier modulation techniques.

MAPPING OF COURSE OUTCOMES (COs) WITH LIST OF EXPERIMENTS:

Exp. No.	Experiments Title	CO's
1.	Design, implementation and study of all the properties of 7-length and 15-length **PN** sequences using shift register.	1
2.	Study of Pulse Amplitude Modulation and Demodulation	2
3.	Study of Pulse Code Modulation and Demodulation	2,4
4.	Study of line coders: polar/unipolar/bipolar NRZ, RZ and Manchester.	3
5.	Study of Delta Modulator and Demodulator.	2,4
6.	Study of Adaptive Delta Modulator and Demodulator.	2,4
7.	Study of BPSK Modulator and Demodulator.	2,5
8.	Study of BFSK Modulator and Demodulator.	2,5
9.	Study of ASK modulator and demodulator.	2,5
10.	Study of QPSK Modulator and Demodulator.	2,5
11.	Simulation study of probability of symbol error for BPSK modulation.	6
12.	Simulation study of probability of symbol error for BFSK modulation.	6
Content beyond the syllabus		
1	Study of Time Division Multiplexing and De multiplexing techniques.	2

MAPPING OF COURSE OUTCOMES (COs) WITH PROGRAM OUTCOMES(POs):

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	2	2	1	2	1	2	1	2	3
CO2	3	2	1	2	2	1	2	1	2	1	2	3
CO3	3	2	1	2	2	1	2	1	2	1	2	3
CO4	3	2	1	2	2	1	2	1	2	1	2	3
CO5	3	2	1	2	2	1	2	1	2	1	2	3
CO6	3	2	1	2	2	1	2	1	2	1	2	3
AVG.	3	2	1	2	2	1	2	1	2	1	2	3

MAPPING OF COURSE OUTCOMES (COs) WITH PROGRAM SPECIFIC OUTCOMES (PSOs):

	PSO-1	PSO-2
CO1	3	3
CO2	3	3
CO3	3	3
CO4	3	3
CO5	3	3
CO6	3	3

Contents

Introduction

This first laboratory in Digital communication has the objective to familiarize the student with the circuit, experiment kit, oscilloscope reading and handling of different instrument related to experiment. Another goal is to reinforce theoretical knowledge with practice and vice-versa, and also to learn correct laboratory procedures and techniques. This is accomplished by building, testing and taking measurements on circuits.

In the execution of the experiments, highest benefit is gained if someone can distinguish between performing the experiment by following step by step instruction, and actually understanding the reasons and methodology. To understand the experiments, theory of the circuit must be understood and to convey the results a correct laboratory report is to be learnt to write.

Guidelines for Laboratory Notebook

The laboratory notebook is a record of all work pertaining to the experiment. Organization in notebook is important. Descriptive heading should be used to separate and identify the various parts of the experiment. A neat, organized and complete record of an experiment is just as important as the experimental work.

- ***For Hardware based Experiments:***

1. **Heading:** The experiment identification (number) should be at the top of each page.

2. **Title:** The name of the experiment.

3. **Objective:** A brief but complete statement of what to find out or verify in the experiment should be at the beginning of each experiment.

4. **Theory:** A brief theory of the experiment should be written in report.

5. **Apparatus Required:** Laboratory equipment refers to the various tools and equipment used in a laboratory for experiment. The laboratory apparatus depends upon the type of laboratory you are in and the experiment you are going to perform.

6. **Block/Connection Diagram:** Always use the simplest diagrams that will serve the purpose. Often this will mean drawing them specifically for the report, rather than reproducing existing diagrams. Each diagram should have a figure number and a caption and should be referred to in the text.

7. **Procedure:** How to perform the experiment. In general, lengthy explanations of procedure are unnecessary. Short commentaries alongside the data may be used.

8. **Graphs / Waveform / Figures:** Figures are used to present large amounts of data in concise visual form. Each curve if more than one on a graph should be labelled.

9. **Analysis and Results:** This section should summarize and display the results of the experiment. This section should be purely factual, where the results are displayed primarily in the form of graphs. Describe the results clearly and concisely .The results should be presented in a form which makes the interpretation easy. Theoretical and experimental results should be on the same graph or arrange in the same table in a way for easy correlation of these results.

10. **Conclusion:** This is the interpretation of results of the experiment as an engineer or designer and should be brief and specific.

- ***For Software based Experiments:***

Heading: The experiment identification (number) should be at the top of each page.

1. **Title:** The name of the experiment.

2. **Aim:** A brief but complete statement of what to find out or verify in the experiment should be at the beginning of each experiment.

3. **Theory:** A brief theory of the experiment should be written in report.

4. **Procedure:** How to perform the experiment. In general, lengthy explanations of procedure are unnecessary. Short commentaries alongside the data may be used.

5. **Algorithm:** Write the algorithm of the program.

6. **MATLAB Code:** Write the MATLAB program.

7. **Graphs / Waveform / Figures:** Figures are used to present large amounts of data in concise visual form. Each curve if more than one on a graph should be labelled.

8. **Results:** The results should be presented in a form which makes the interpretation easy. Theoretical and experimental results should be on the same graph or arrange in the same table in a way for easy correlation of these results.

9. **Conclusion:** This is the interpretation of results of the experiment as an engineer or designer and should be brief and specific.

EXPERIMENT # 1

Title: STUDY OF PCM AND DEMODULATION

Objective:

- PCM and Demodulation

Theory:

A pulse code modulator converts an analog signal to digital form and encodes the signal into any equivalent form such as binary wave form.
The analog signal is sampled according to the Nyquist criteria. The nyquistcriteria states that 'for faithful reproduction of the band limited signal, the sampling rate must be at least twice the highest frequency component present in the signal.' For audio signals the highest frequency component is 3.4 KHz.

So, *Sampling Frequency* ≥2 fm
≥2 x 3.4 KHz
≥6.8 KHz

Practically, the sampling frequency is kept slightly more than the required rate.
Each binary word defines a particular narrow range of amplitude level. The sampled value is then approximated to the nearest amplitude level. The sample is then assigned a code corresponding to the amplitude level, which is then transmitted. This process is called as *Quantization* & it is generally carried out by the A/D converter.
If a signal lies in the range (- m_p , m_p) which is partitioned into ' L' intervals then magnitude of each level 'Δ' is[m_p – (- m_p)] / L or 2m_p/ L.

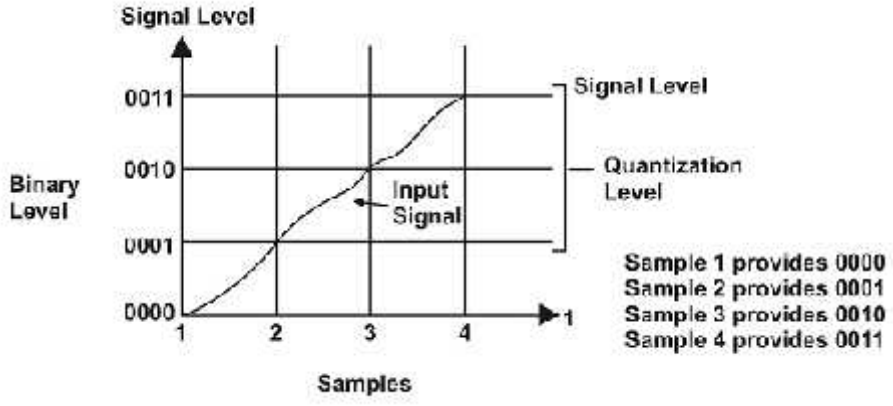


Fig. 1.1

The sample & hold circuitry holds the sample value till the next sample.
Typically A/D converter gives binary output in parallel form. Hence the block schematic of a PCM system is shown in figure. The parallel output from A/D converter is converted into serial form by a parallel to serial converter whose output is a serial output stream. In a digital communication system such signals from serial subscribers are multiplexed, modulated and transmitted over a channel to the destination. At the destination after demultiplexing, demodulation and detection, the signals are fed into a PCM receiver. So the PCM receiver converts the serial signals into parallel form using a serial to parallel form one signals sample at a time and parallel output is

stored into a latch. So the parallel out puts then fed to a D/A converter, to convert the digital signal into an analog equivalent. The analog output is passed through a low pass filter to get a smooth output. The parallel to serial converter, a serial to parallel converter, latch and A/D converter requires timing signals for operation.
The process of quantization introduces quantization noise except for which the output sample is equal to the input at the sampling instances also it is closely equal to the input signal within the linearity range.

ST2153 &ST2154:

Apparatus Required:

- Pulse Code Mod./Demod. Experiment Kit (ST2153 &ST2154).
- Digital Multimeter.
- A CRO / DSO

Block/Connection Diagram:

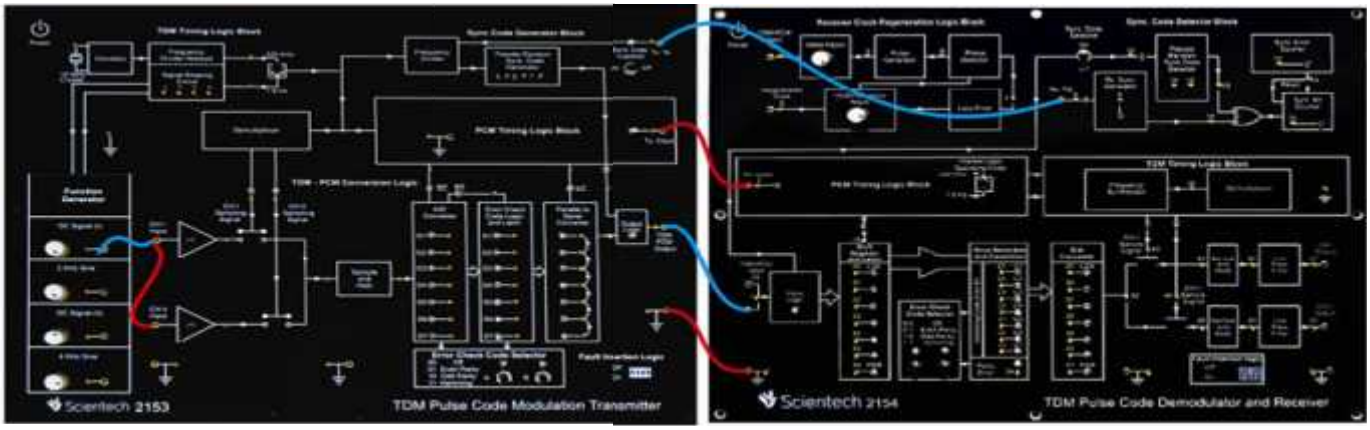


Fig. 1.2

Procedure:

1. Connect the circuit as shown in Figure 1.2.
2. Vary and measure the D.C. input from + 5V to – 5V in steps of 1V with the help of amplitude control knob in DC source.
3. Observe the output on the A/D converter block LED's (D1 to D7). The LED's represent the state of the binary PCM word allocated to the PAM sample being processed. An illuminated LED represent a '1' state, while non-illuminated LED indicates a '0' state.
   D7 is the MSB & D1 is the LSB. The LED output looks as follows.

D7	D6	D5	D4	D3	D2	D3	D2	D1
1	0	0	0	0	0	0	0	0

This output is the digital representation of **0**V input to CH.1

4. Feed the PCM data to the Receiver (demodulator circuit) as shown in figure 1.2 and observe the output at the output of D/A which is quantized level. Measure the voltage by multimeter at the output (TP 41 and TP 50) of low-pass filter for the DC signals transmission.
5. Using multimeter /scope and compare it with the original signal and you can observe that the loss ininformation in process of conversion and transmission.
6. Plot an input - output curve to observe the effect of quantization (de-quantization) error. A graphical example is shown in Fig.1.3 for few values.

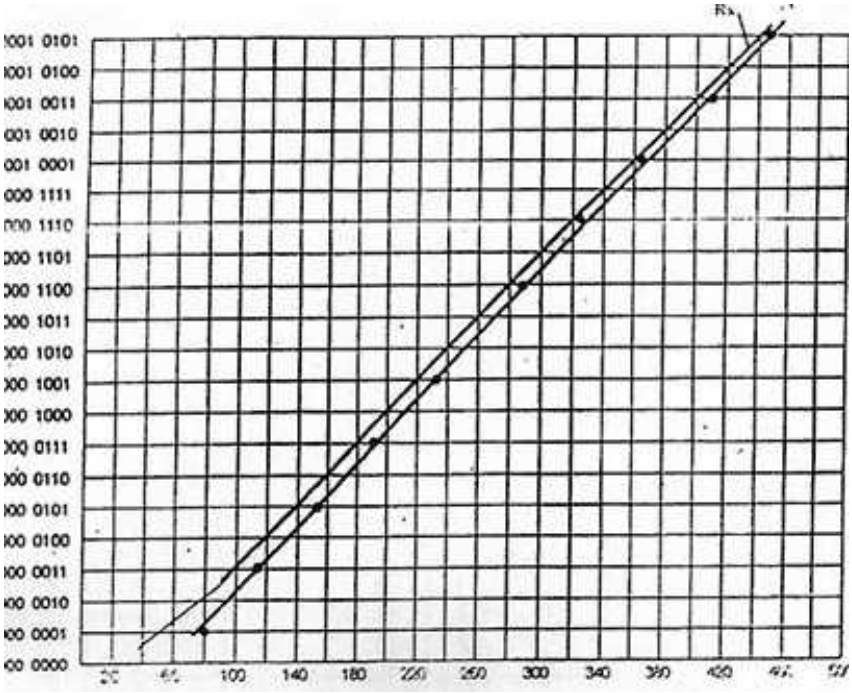


Fig.1.3

Experimental Data:

Table 1

Transmitter Section:

DC I/P Voltage	Encoded Values (Theo.)							Encoded Values (Pr.)						
	D7	D6	D5	D4	D3	D2	D1	D7	D6	D5	D4	D3	D2	D1
-5	0	0	0	0	0	0	0							
-4														
-3														
-2														
-1														
0	1	0	0	0	0	0	0							
1														
2														
3														
4														
5	1	1	1	1	1	1	1							

Table 2

Receiver Section:

DC I/P Voltage	Decoded Values (Theo.)							Decoded Values (Pr.)							DC O/P Voltage
	D7	D6	D5	D4	D3	D2	D1	D7	D6	D5	D4	D3	D2	D1	
-5															
-4															
-3															
-2															
-1															
0															
1															
2															
3															
4															
5															

ME 751:

STUDY OF PCM AND DEMODULATION

Block/Connection Diagram:

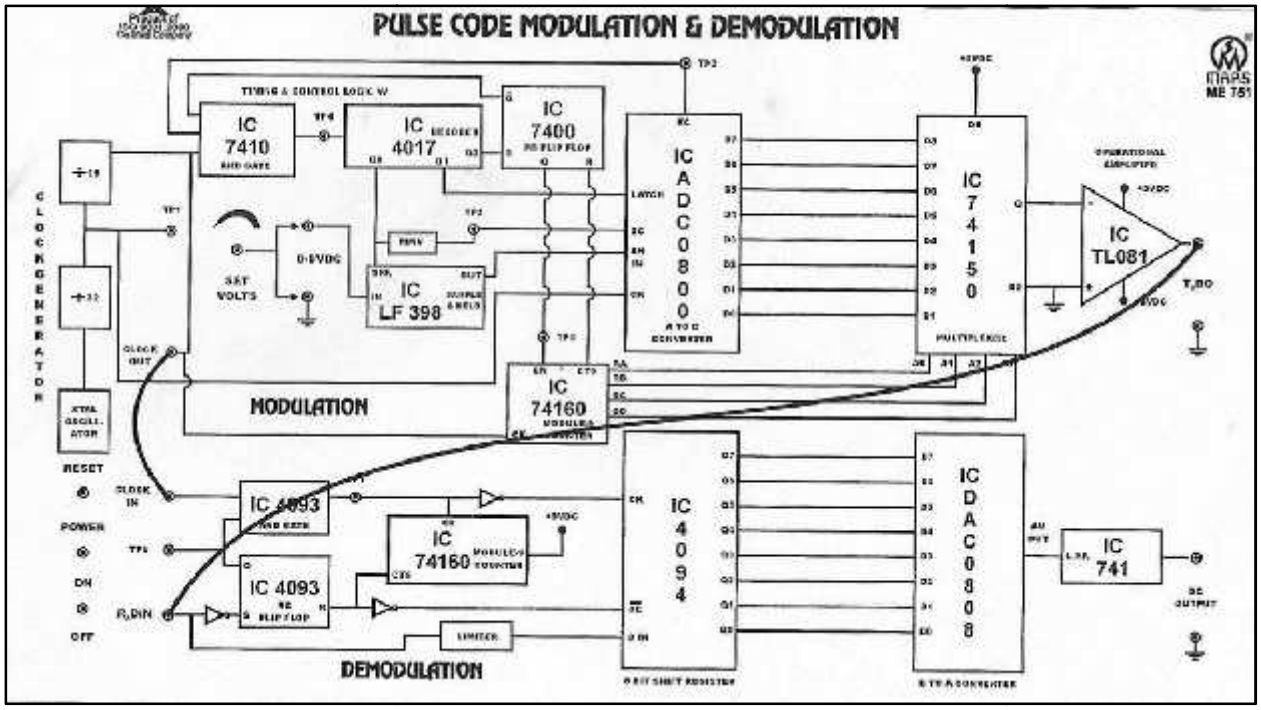


Fig. 1.4

Procedure:

1. Connect the circuit as shown in Figure 1.4. and connect a digital multimeter across the sockets '0 – 5V DC'.
2. Increase the D.C. voltage from 0V to 5V in steps of 1V with the help of amplitude control knob in DC source.
3. Observe the output on the A/D converter block LED's (D1 to D7). The LED's represent the state of the binary PCM word allocated to the PAM sample being processed. An illuminated LED represent a '1' state, while non-illuminated LED indicates a '0' state.
   D7 is the MSB & D0 is the LSB.
4. Feed (TxD0 to RxDIN) the PCM data to the Receiver (demodulation circuit) as shown in figure 1.4 and observe the output at the output of D/A which is quantized level. Measure the voltage by multimeter at the DC output.
5. Using multimeter, compare it with the original signal and you can observe that the loss in information in process of conversion and transmission.

6. Plot an input - output curve to observe the effect of quantization (de-quantization) error. A graphical example is shown in Fig.1.5for few values.

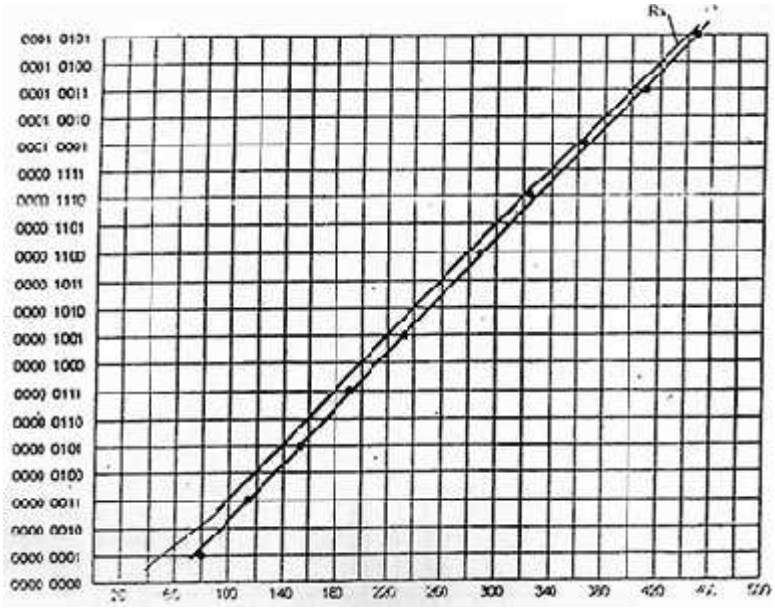


Fig. 1.5

Experimental Data:

Table 1

Transmitter Section:

DC I/P Voltage	Encoded Values (Theo.)								Encoded Values (Pr.)							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
5	1	1	1	1	1	1	1	1								
4																
3																
2																
1																
0	0	0	0	0	0	0	0	0								

Table 2

Receiver Section:

DC I/P Voltage	Decoded Values (Theo.)								Decoded Values (Pr.)								DC O/P Voltage
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	
5																	
4																	
3																	
2																	
1																	
0																	

Data Analysis:

1. Tally the equivalent binary value of input analog voltage with the binary value available at the output of ADC. Calculate the percentage error if any.
2. Tally the binary bit pattern available at the output of DAC with the output available at DAC.

Discussion:

Write briefly your comments about the above experiment.

Precautionary Measure to be taken:

1. Ensure that equipment or training kit switch is kept off. While connecting it to main power supply.
2. For connecting any signal from one equipment to another equipment or from one section to other section of the same kit, ensure that signal is grounded properly and subsequently connect the signal-to-signal line.
3. Handle gently all the necessary button or knob in the equipment avoiding all other buttons or knobs which are not required to be adjusted for the equipment.
4. For unusual spark or burning smell, immediately switch off the main supply to the kit.
5. Ensure that, a signal is connected to an appropriate junction destined for it.
6. Always cover the equipment for dust protection after the experiment.

Some Sample questions:

1. Design a PCM system taking input analog voltage starting from 0.5 V and increasing in steps of 0.5 V up to 5 V. Take the binary bit pattern at modulated output.
2. For the above question calculate the error between input analog voltage and output analog voltage.

EXPERIMENT # 2

Title: STUDY OF LINE CODERS

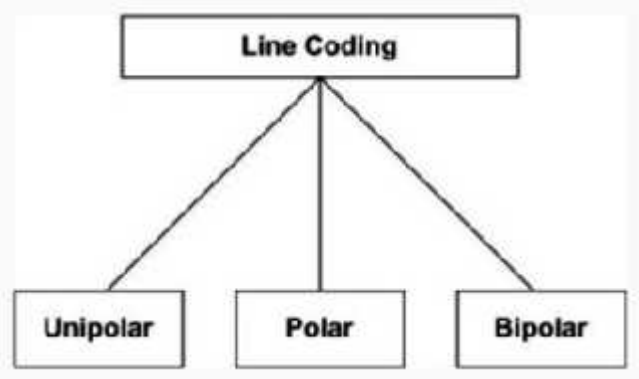
Objective:

- Study of **data formats**: NRZ (L), NRZ (M), RZ, AMI, RB,Biphase (Manchester), Biphase (Mark).

Theory:

Line coding consists of representing the digital signal to be transported, by an amplitude- and time-discrete signal that is optimally tuned for the specific properties of the physical channel (and of the receiving equipment). The waveform pattern of voltage or current used to represent the 1s and 0s of a digital signal on a transmission link is called line encoding. The common types of line encoding are Unipolar, Polar, Bipolar NRZ, RZand Manchester encoding.
We can roughly divide line coding schemes into three categories:

1. Unipolar (e.g.NRZ, RZ).
2. Polar (e.g. NRZ-L, NRZ-I, RZ, and Biphase – Manchester and differential Manchester).
3. Bipolar (e.g.RB, AMI and Pseudoternary).



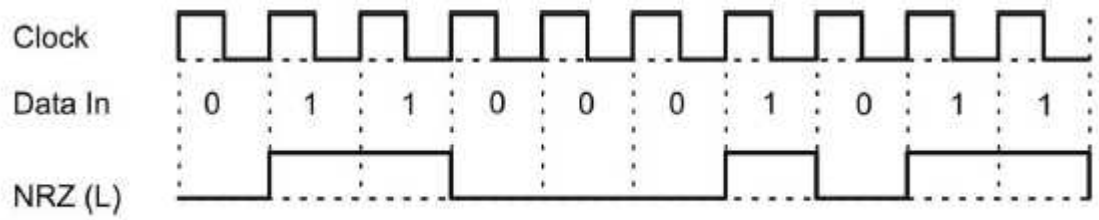
Unipolar scheme: In unipolar encoding technique, only two voltage levels are used. It uses only one polarity of voltage level i.e.,all the signal levels are either above or below the axis.
Polar schemes: Polar encoding technique uses two voltage levels – one positive and the other one negative i.e., the voltages are on the both sides of the axis.
Bipolar schemes: The term **bipolar** signaling is used by some authors to designate a specific line coding scheme with positive, negative, and zero voltage levels. The voltage level for one data element is at zero, while the voltage level for the other element alternates betweenpositive and negative.
There are several possible ways of assigning waveforms (pulses) to the digital data. In the binary case (two symbols), for example, conceptually the simplest line code is **on-off**, where 1 is transmitted by a pulse and 0 is transmitted by no pulse (zero signal).
There are two common forms of level line codes: one is called **returnto zero (RZ)** and the other is called **non-returntozero(NRZ).** In RZ coding, the level of the pulse returns to zero for

a portion of the bit interval. In NRZ coding, the level of the pulse is maintained during the entire bit interval.

Line coding formats are further classified according to the polarity of the voltage levels used to represent the data. If only one polarity of voltage level is used, i.e., positive or negative (in addition to the zero level) then it is called **unipolar** signaling. If both positive and negative voltage levels are being used, with or without a zero voltage level, then it is called **polar** signaling. The term**bipolar** signaling is used by some authors to designate a specific line coding scheme with positive, negative, and zero voltage levels.

A. Non-Return to Zero - Level (NRZ-L):

This is the most extensively used waveform in digital logics. The data format is very simple where all 'ones' are represented by 'high' and all 'zeros' by 'low'. The data format is directly available at the output of all digital data generation logics and hence very easy to generate. Here all the transitions take place at the rising edge of the clock.

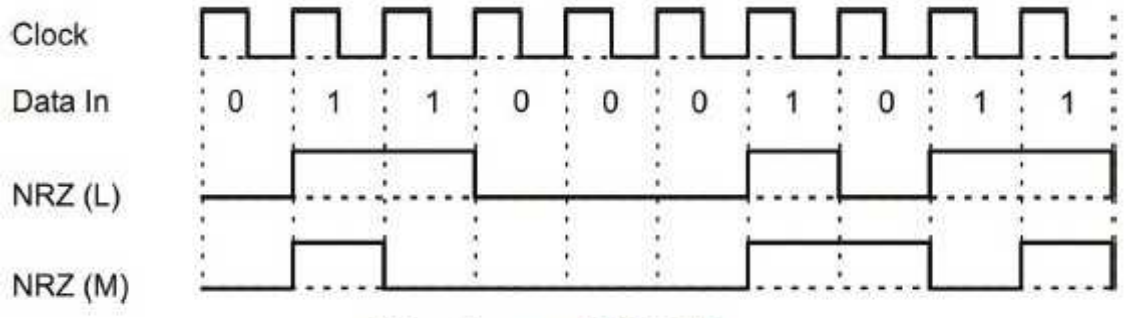


Waveforms of NRZ-L

Fig.2.2

B. Non-Return to Zero - Mark (NRZ-M):

This type of line code uses an inversion (I) to designate binary digits, specifically, a change in level or no change in level. There are two variants of this code, NRZmark (M) and NRZspace (S). In NRZ (M), a change of level is used to indicate a binary **1,** and no change of level is used to indicate a binary **0.** In NRZ (S) a change of level is used to indicate a binary **0,** and no change of level is used to indicate a binary **1.**The transitions take place at the rising edge of the clock.



Waveforms of NRZ-M

Fig.2.3

C. Non-Return to Zero - Space (NRZ-S):

This type of waveform is marked by change in levels for 'zeros' and no transition for 'ones' and the transitions take place at the rising edge of the clock.

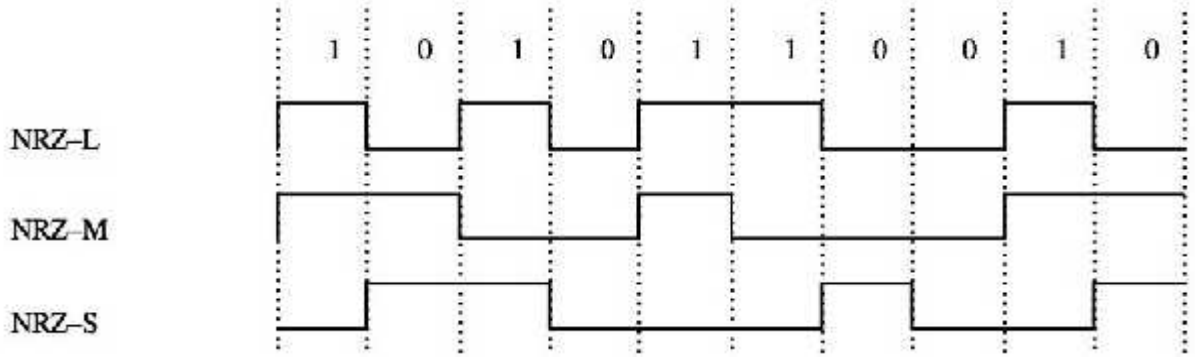
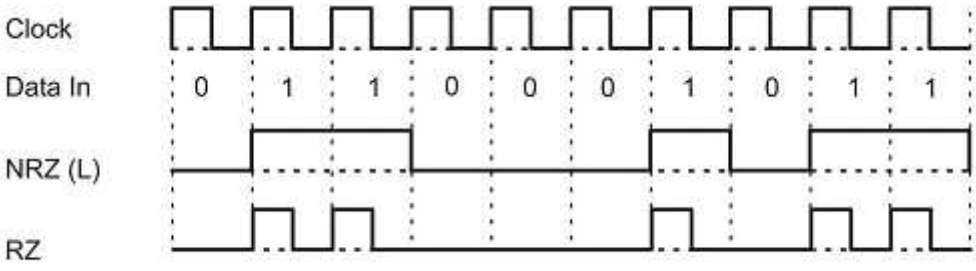


Fig.2.4

D. Unipolar Return to Zero (RZ):

In this type of unipolar signaling, a High in data, though represented by a **Mark pulse**, its duration T_0 is less than the symbol bit duration. Half of the bit duration remains high but it immediately returns to zero and shows the absence of pulse during the remaining half of the bit duration.

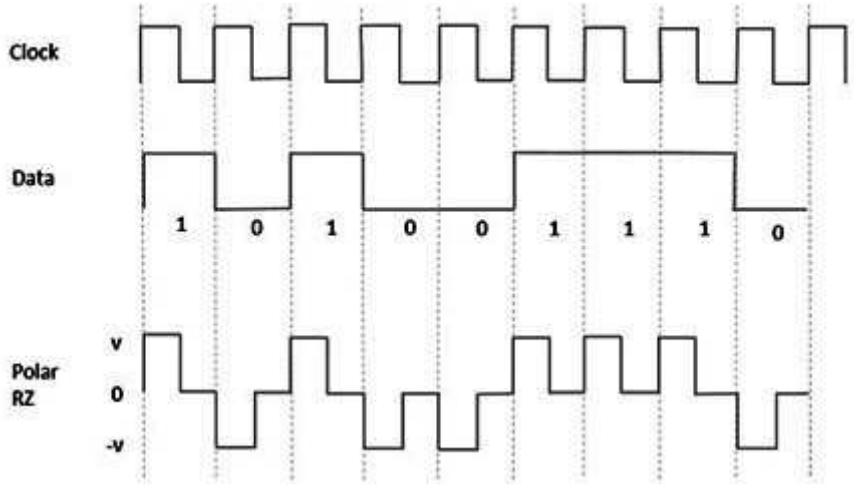


Waveforms of RZ-L

E. Polar Return to Zero (RZ):

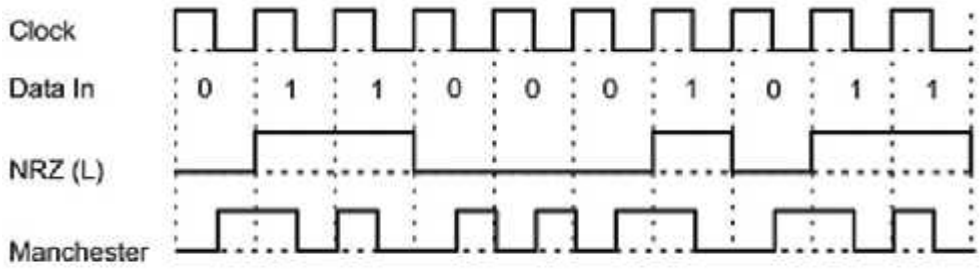
In this type of Polar signaling, a High in data, though represented by a **Mark pulse**, its duration T_0 is less than the symbol bit duration. Half of the bit duration remains high but it immediately returns to zero and shows the absence of pulse during the remaining half of the bit duration.

However, for a Low input, a negative pulse represents the data, and the zero level remains same for the other half of the bit duration. The following figure depicts this clearly.



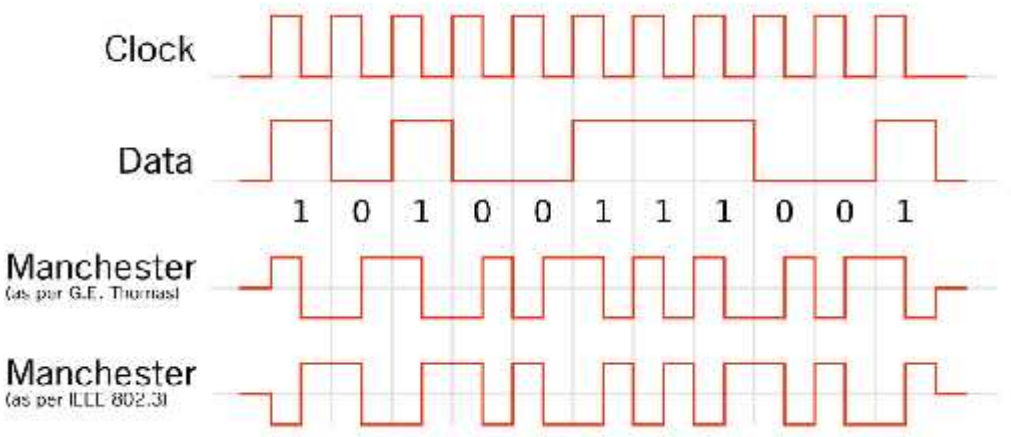
F. Biphase (Manchester):

In this type of coding, the transition is done at the middle of the bit-interval. The transition for the resultant pulse is from High to Low in the middle of the interval, for the input bit 1. While the transition is from Low to High for the input bit **0**.
For bit 1, +5V for first half bit time and 0V during the second half and for bit 0, 0V for first half bit time and +5V during the second half.
Manchester encodings have transitions in the middle of the clock cycle, with the type depending on the encoding. Manchester is an NRZ encoding that is exclusively-ORed with the clock. This provides at least one transition per bit.



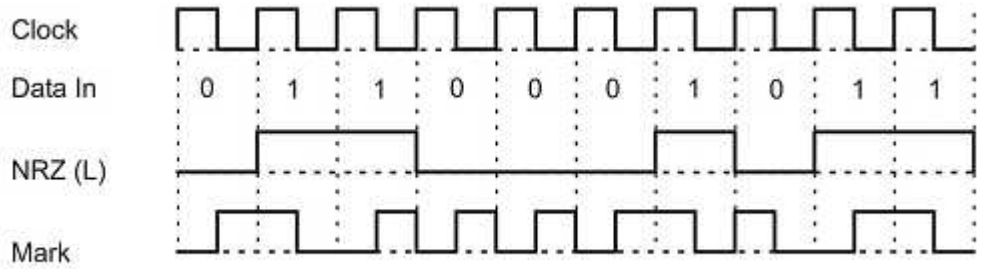
Waveforms of Manchester

An example of **Manchester encoding** showing both conventions:



G. Biphase (Mark):

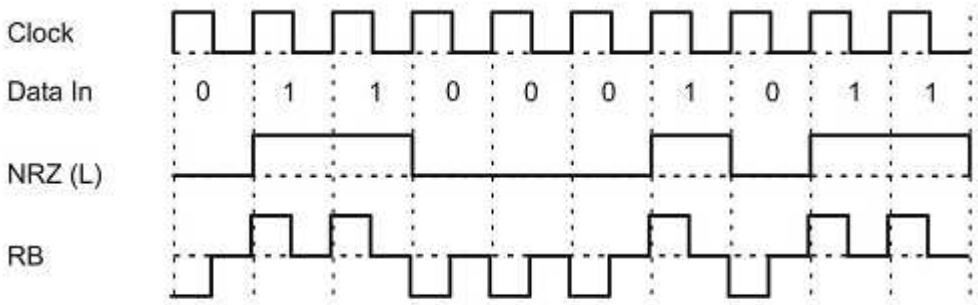
In this type of coding, Level change occurs at the beginning of every bit period "One" is represented by a midbit level change "Zero" is represented by no midbit level change.
For any bit either 1 or 0, first half bit duration +5V or 0V and inverts of first half during next half bit duration.



Waveforms of Mark

H. Return to Bias (RB):

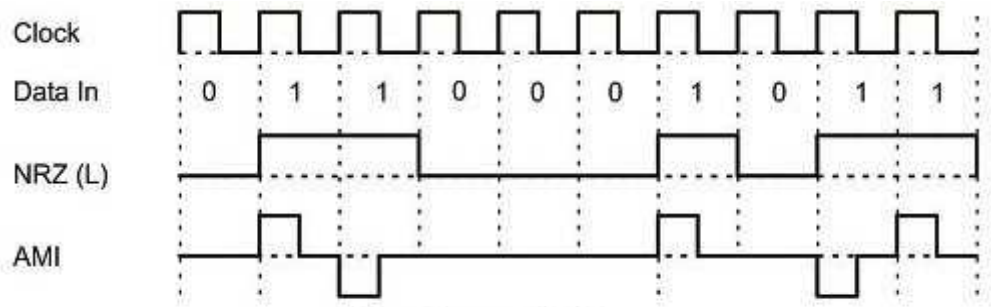
In this type of coding, during the first half a period, positive level for bit 1 and a negative level for bit 0 and during the second half bit time, both returns to the bias level.



Waveforms of RB

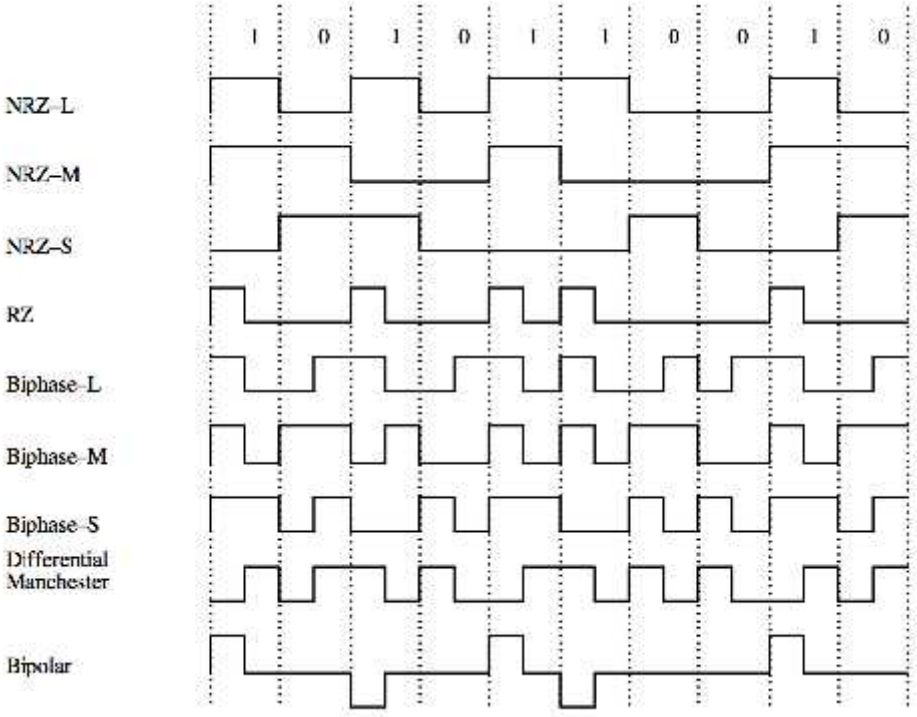
I. Alternate Mark Inversion (AMI):

In this type of coding, a zero is sent as a 0 while a one is sent as either a positive voltage or negative, which alternates. So a 1 is sent as one polarity and then the opposite polarity.
Like RB encoding, the AMI always returns to the bias level during second half of the bit time interval and during the first half the transmitted level can be a positive, a negative or bias level, as for a bit 0 bias level and for a bit 1 either a positive level or negative level, the level being chose opposite to what it was used to represent the previous bit 1.



Waveforms of AMI

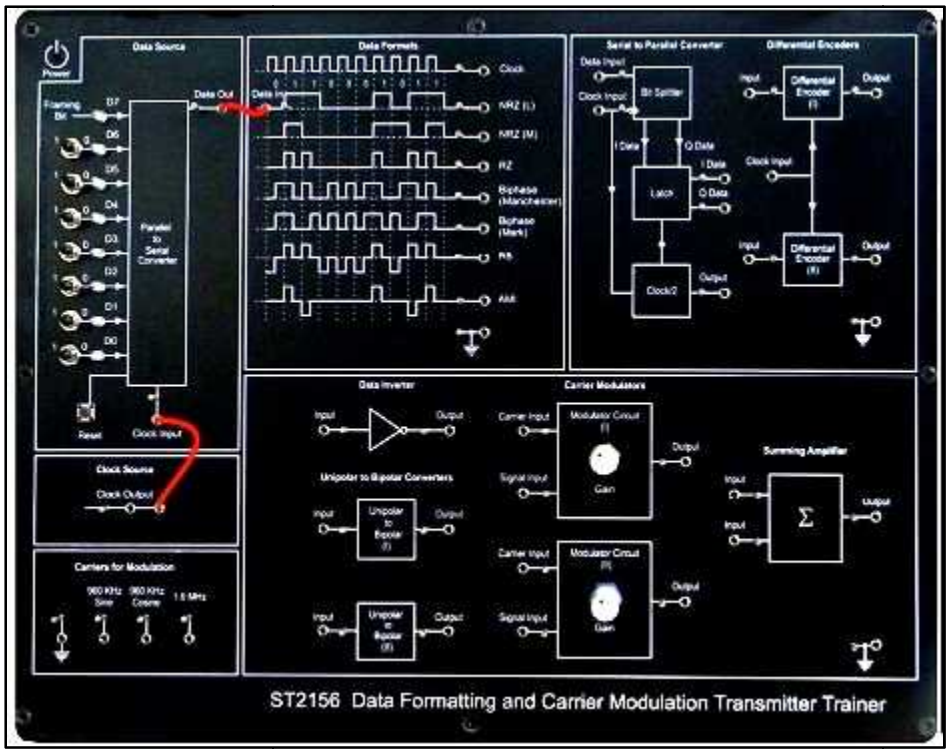
Example of different coding:



Apparatus Required:

- Line CodersKit (ST2156 & ST2157).
- A CRO / DSO

Block/Connection Diagram:



Procedure:

1. Connect the power supply of ST2156 but do not turn on the power supplies until connections are made for this experiment.
2. Make the connections as shown in the figure.
3. Switch 'ON' the power.
4. Connect oscilloscope CH1 to 'Data In' and CH2 to 'Clock In' and observe the waveforms.
5. Connect oscilloscope CH1 to 'Data In' and CH2 to 'NRZ (L)' and observe the waveforms.
6. Connect oscilloscope CH1 to 'Data In' and CH2 to 'NRZ (M)' and observe the waveforms.
7. Connect oscilloscope CH1 to 'Data In' and CH2 to 'RZ' and observe the waveforms.
8. Connect oscilloscope CH1 to 'Data In' and CH2 to 'Biphase (manchester)'and observe the waveforms.
9. Connect oscilloscope CH1 to 'Data In' and CH2 to 'Biphase (Mark)' and observe the waveforms.
10. Connect oscilloscope CH1 to 'Data In' and CH2 to 'RB' and observe the waveforms.
11. Connect oscilloscope CH1 to 'Data In' and CH2 to 'AMI' and observe the waveforms.

Observations:

1. The output at 'Data In' is repeating sequence of bits generated by Parallel to serial Converter.
2. The 'NRZ (L)' data is same as 'Data In' but it is one bit shifted.
3. Verify all the formatting techniques according to example patterns given on the ST2156 board.

Conclusions:

1. The NRZ(L) waveform simply goes low for one bit time to represent a data '0' and high for one bit time to represent a data '1'.
2. In the NRZ (M) line codes the present level is related to the previous level that is when logic '1' is to be transmitted change in level occurs and for logic '0' the level remains unchanged.
3. In the RZ line codes, the maximum signal frequency of 'RZ' signal occurs when a string of '1' is transmitted. It is equivalent to sending two logic levels in each clock period. Thus bandwidth requires is twice as that required for the NRZ waveforms.
4. The Biphase Manchester codes always contain at least one transition per bit time, irrespective of the data being transmitted. Hence the maximum frequency of the biphase code is equal to the data clock rate when a stream of consecutive data '1' & '0' is transmitted. Therefore the required bandwidth is same as that of RZ code & double as that of NRZ (L) code.
5. In the 'Biphase Mark' if a data '0' is to be transmitted, the sequence of the transmitted levels will remain same as for the previous bit interval and if a '1' is to be transmitted , the sequence of the transmitted levels will reverse i.e. phase reversal will occur.
6. The Biphase Mark code being very similar to the Biphase (Manchester) coding requires same amount of bandwidth which is double as that of NRZ (L).
7. The maximum signal frequency in RB code is equal to the data clock frequency, the bandwidth requirements is same as that for RZ, Biphase codes and double that for NRZ codes.
8. The maximum transition rate for AMI can only occur during a stream of all '1s' thus the bandwidth required is twice that required for the NRZ codes.

Discussion:

Write briefly your comments about the above experiment.

Precautionary Measure to be taken:

1. Ensure that equipment or training kit switch is kept off. While connecting it to main power supply.

2. For connecting any signal from one equipment to another equipment or from one section to other section of the same kit, ensure that signal is grounded properly and subsequently connect the signal-to-signal line.
3. Handle gently all the necessary button or knob in the equipment avoiding all other buttons or knobs which are not required to be adjusted for the equipment.
4. For unusual spark or burning smell, immediately switch off the main supply to the kit.
5. Ensure that, a signal is connected to an appropriate junction destined for it.
6. Always cover the equipment for dust protection after the experiment.

Some Sample questions:

1. Assume we want to transmit the following binary string: 0110001011. Show the data formats following line coding techniques:
    - NRZ (L)
    - NRZ (M)
    - RZ
    - Biphase (Manchester)
    - Biphase (Mark)
    - AMI
    - RB
2. Show the difference between Unipolar, Polar and Bipolar Line Coding Schemes with examples.

EXPERIMENT # 3

Title: STUDY OF AMPLITUDE SHIFT KEYING

Objective:

- Study of ASK modulator and demodulator.

Theory:

The simplest method of modulating a carrier with a data stream is to change theamplitude of the carrier wave every time the data changes. This modulation techniqueis known as Amplitude Shift Keying.

The simplest way of achieving amplitude shift keying is by switching 'ON' the carrierwhenever the data bit is '1' & switching it 'OFF' whenever the data bit is '0' i.e. thetransmitter outputs the carrier for a' 1 ' & totally suppresses the carrier for a '0'. Thistechnique is also known as ON-OFF keying. Figure 3.1 illustrates the amplitude shiftkeying for the given data stream.

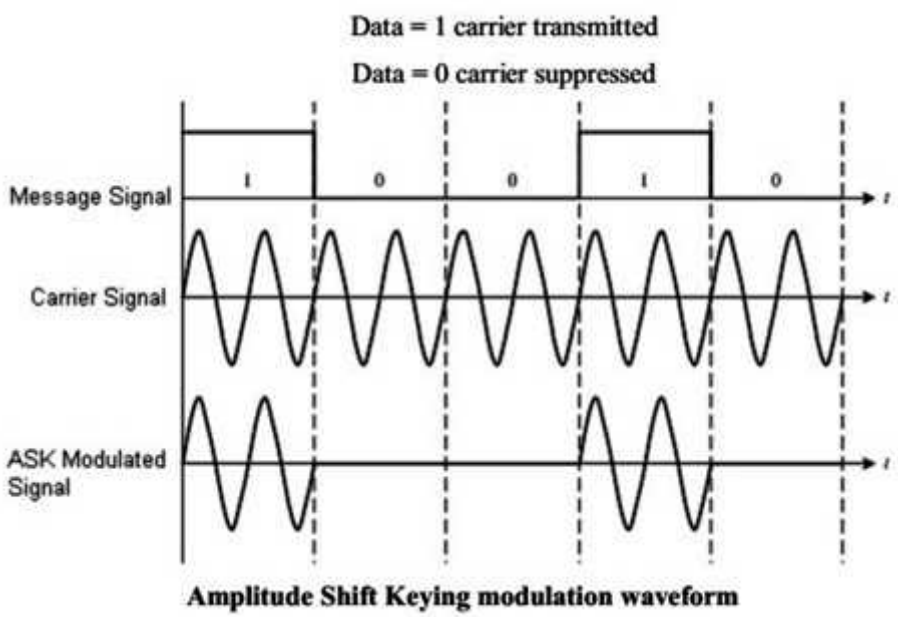


Fig. 3.1

The ASK waveform is generated by a balanced modulator circuit, also known as a linear multiplier. As the name suggests, the device multiplies the instantaneous signal at its two inputs. The output voltage being product of the two input voltages at any instance of time. One of the inputs is AC coupled 'carrier' wave of high frequency. Generally, the carrier wave is a sinusoidal signal since any other waveform would increase the bandwidth. The data stream applied is unipolar i.e. 0 volts for logic '0' & + 5 Volts for logic '1'.The output of balanced modulator is a sine wave, unchanged in phase when a data bit 'I' is applied to it and is zero when the data bit '0' is applied.

The ASK modulation result in a great simplicity at the receiver. The method to demodulate the ASK waveform is to rectify it, pass it through the filter & 'shape up' the resulting waveform. The output is the original data stream.

ST2156 & ST2157

Apparatus Required:

- ASK Mod/DemodKit (ST2156 & ST2157).
- A CRO / DSO

Block/Connection Diagram:

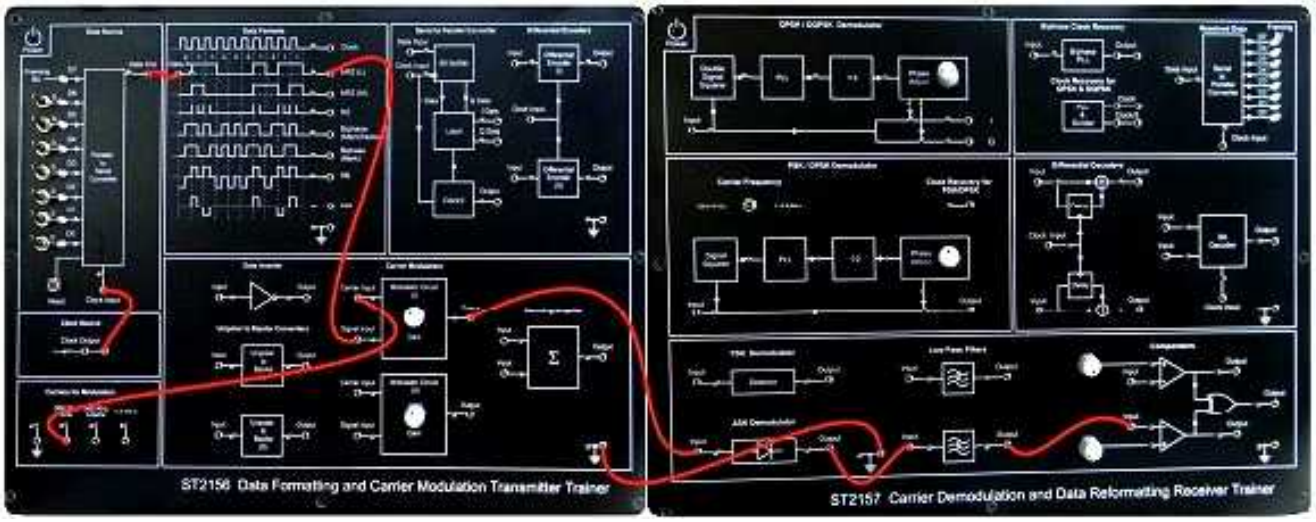


Fig. 3.2

Procedure:

1. Connect the power supplies of ST2156 and ST2157 but do not turn on the power supplies until connections are made for this experiment.
2. Make the connections as shown in the figure 3.2.
3. Switch 'ON' the power.
4. On ST2156, connect oscilloscope CH1 to 'Clock In' and CH2 to 'Data In' and observe the waveforms.
5. On ST2156, connect oscilloscope CH1 to 'NRZ (L)' and CH2 to 'Output' of modulator Circuit (I) on ST2156 and observe the waveforms.
6. Vary the gain potentiometer of modulator circuit (I) on ST2156 to adjust the amplitude of ASK Waveform.
7. On ST2156, connect oscilloscope CH1 to 'NRZ (L)' and CH2 to 'Output' of comparator on ST2157 and observe the waveforms.

Observations:

1. The output at 'Data In' is repeating sequence of bits generated by Data Source.
2. The output at Modulator Circuit (I) is the ASK waveform which contains carrier transmitted for Data '1' and carrier suppressed Data '0'.
3. The output at comparator on ST2157 is the same as 'Data In' on ST2156.

Conclusions:

1. Amplitude shift keying is fairly simple to implement in practice, but it is less efficient, because the noise inherent in the transmission channel can deteriorate the signal so much that the amplitude changes in the modulated carrier wave due to noise addition, may lead to the incorrect decoding at the receiver.
2. The technique is not widely used is practice. Application wise, it is however used in diverse areas and old as emergency radio transmissions and fiber-optic communications.

Discussion:

Write briefly your comments about the above experiment.

SCIENTECH 2807

Apparatus Required:

- ASK Mod/DemodKit (**Scientech 2807**).
- A CRO / DSO

ASK Modulation:

Block Diagram:

ASK Modulator:

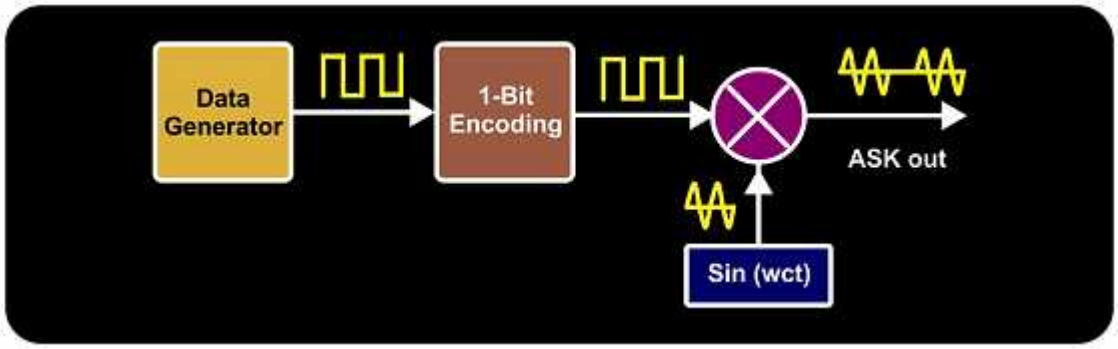


Fig. 3.3

Procedure:

1. Connect and switch on the power supply of Scientech 2807.
2. Select input *Data pattern* using push button i.e. 8-Bit, 16-Bit, 32-Bit, 64- Bit. And respective LED will glow. Observe the input Data on test point (TP2).
3. Select input *data clock* using push button i.e. 2 KHz, 4 KHz, 8 KHz, 16 KHz. Observe the change in frequency on test point (TP1).
4. Observe the change in frequency of carrier signal at (TP4).
5. ASK Modulator is by default selection when switch on the power supply of Scientech 2807 and LED of (TP3) will glow.
6. Observe the ASK modulator output on (TP5).

Observation:

1. Observe the Input Data at TP2.
2. Observe the Input data clock at TP1.
3. Observe the encoded data input at TP3.
4. Observe the Carrier signal at TP4.
5. Observe the Modulated output at TP5.
6. Observe the following data Patterns on TP2
   - 8-Bit: "10110010"
   - 16-Bit: "0100110110110010"
   - 32-Bit: "00000101000101111100101000111111"
   - 32-Bit:"10101100111000111110000111111000000111110000111000110010101000111010"

ASK Demodulation:

Block Diagram:

ASK Demodulator:

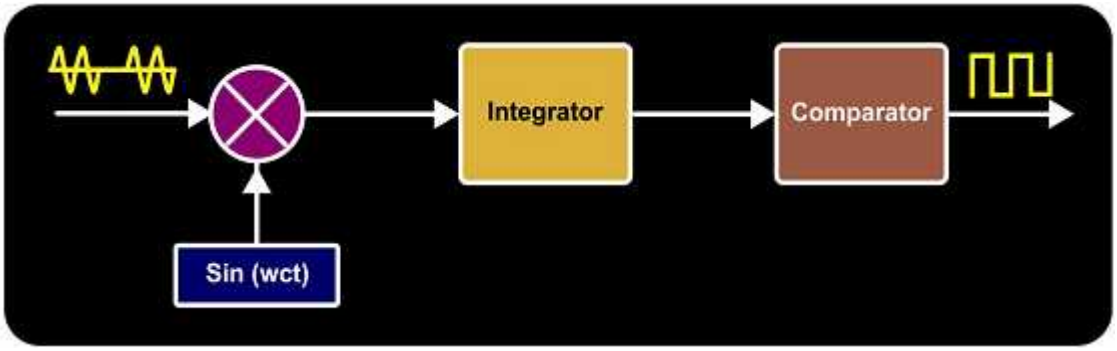


Fig. 3.4

Procedure:

1. Connect and switch on the power supply of Scientech 2807.
2. Select input *Data pattern* using push button i.e. 8-Bit, 16-Bit, 32-Bit, 64-Bit. And respective LED will glow. Observe the input Data on test point (TP2).
3. Select input *data clock* using push button i.e. 2 KHz, 4 KHz, 8 KHz, 16 KHz. Observe the change in frequency on test point (TP1).
4. Observe the change in frequency of carrier signal at (TP4).
5. ASK Modulator is by default selection when switch on the power supply of Scientech 2807 and LED of (TP3) will glow.

Observation:

1. Observe the Input Data at TP2.
2. Observe the Input data clock at TP1.
3. Observe the 1-bit encoded input data at TP3.
4. Observe the Carrier signal at TP4 and TP6.
5. Observe the Modulated output at TP5.
6. Observe the multiplier output at TP7
7. Observe the Integrator output at TP8
8. Observe the output at TP9
9. Observe the following data Patterns on TP2
   - 8-Bit: "10110010"
   - 16-Bit: "0100110110110010"
   - 32-Bit: "00000101000101111100101000111111"
   - 32-Bit: "10101100111000111100001111100000111110000011100011001010100011110 10"

*Note: If output at any TP does not appear proper then Press **RESET** button.

Discussion:

Write briefly your comments about the above experiment.

Precautionary Measure to be taken:

1. Ensure that equipment or training kit switch is kept off. While connecting it to main power supply.
2. For connecting any signal from one equipment to another equipment or from one section to other section of the same kit, ensure that signal is grounded properly and subsequently connect the signal-to-signal line.
3. Handle gently all the necessary button or knob in the equipment avoiding all other buttons or knobs which are not required to be adjusted for the equipment.
4. For unusual spark or burning smell, immediately switch off the main supply to the kit.
5. Ensure that, a signal is connected to an appropriate junction destined for it.
6. Always cover the equipment for dust protection after the experiment.

Some Sample questions:

1. Why is ASK called as ON-OFF keying
2. Implement a system to transmit and receive a binary stream using **ASK** scheme and trace the waveforms. Measure the related amplitudes and frequencies.
3. What is the major problem of ASK modulation in wireless transmission?

EXPERIMENT # 4

Title: STUDY OF FREQUENCY SHIFT KEYING

Objective:

- Study of FSK modulator and demodulator.

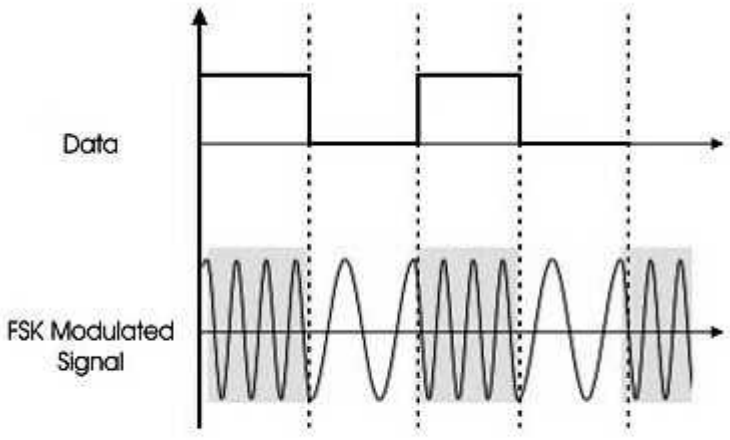
Theory:

Frequency shift keying (FSK) is a digital modulation scheme, which is similar to the frequency modulation (FM). In a digital communication system, the sources produce digital signals. A binary source produces a random sequence of '0's and '1's. A quaternary source produces a random sequence of '0's, '1's, '2's and '3's. Similarly, high level (m – symbol) sources produce m – array signals.

In the m – array FSK modulation scheme, the input digital signal is used to switch the carrier frequency between m – different frequencies depending the symbol. In binary communication, the carrier frequency is switched between two levels – f_0 and f_1.

This scheme is widely used in data communications, particularly voice band communication using modems.

In frequency shift keying, the carrier frequency is shifted in steps (i.e. from one frequency to another) corresponding to the digital modulation signal. If the higher frequency is used to represent data '1' & lower frequency for data '0', the resulting Frequency shift keying waveform appears as shown in figure 4.1.



Frequency Shift Keying Waveform

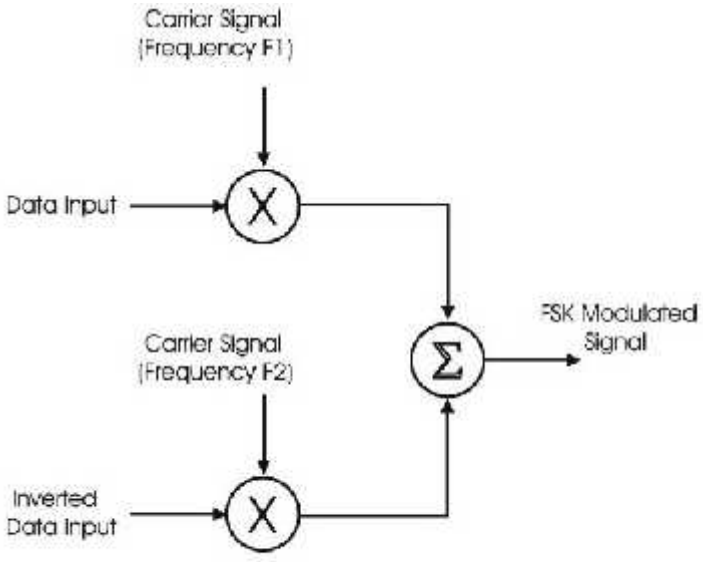
Fig.4.1

The FSK signal can be expressed as

X (t) = A cos ($2\omega_1 t + \theta$), when the data bit is a '1'.

= A cos ($2\omega_0 t + \theta$), when the data bit is a '0' .Where $\omega_1 = 2\Pi f_1$ and $\omega_0 = 2\Pi f_0$

The functional blocks required in order to generate the FSK signal is as shown in figure 4.2. There are two ASK modulator, each has different carrier frequencies but the digital data is inverted in one of the modulator. These two different ASK modulated signal are applied to the summing amplifier to get FSK modulated signal.



Frequency Shift Keying Modulator

Fig.4.2

In **ST2157** the demodulation of FSK waveform can be carried out by a phase locked loop. As known, the phase locked loop tries to 'lock' to the input frequency. It achieves this by generating corresponding output voltage to be fed to the voltage controlled oscillator, if any frequency deviation at its input is encountered. Thus the PLL detector follows the frequency changes & generates proportional output voltage. The output voltage from PLL contains the carrier components. Therefore the signal is passed through the low pass filter to remove them. The resulting wave is rounded to be used for digital data processing. Also, the amplitude level may be very low due to channel attenuation. The signal is 'Shaped Up' by feeding it to the voltage comparator. The functional block diagram of FSK demodulator is shown in figure 4.3.

Frequency Shift Keying Demodulator

Fig.4.3

ST2156 & ST2157

Apparatus Required:

- FSK Mod/DemodKit (ST2156 & ST2157).
- A CRO / DSO

Block/Connection Diagram:

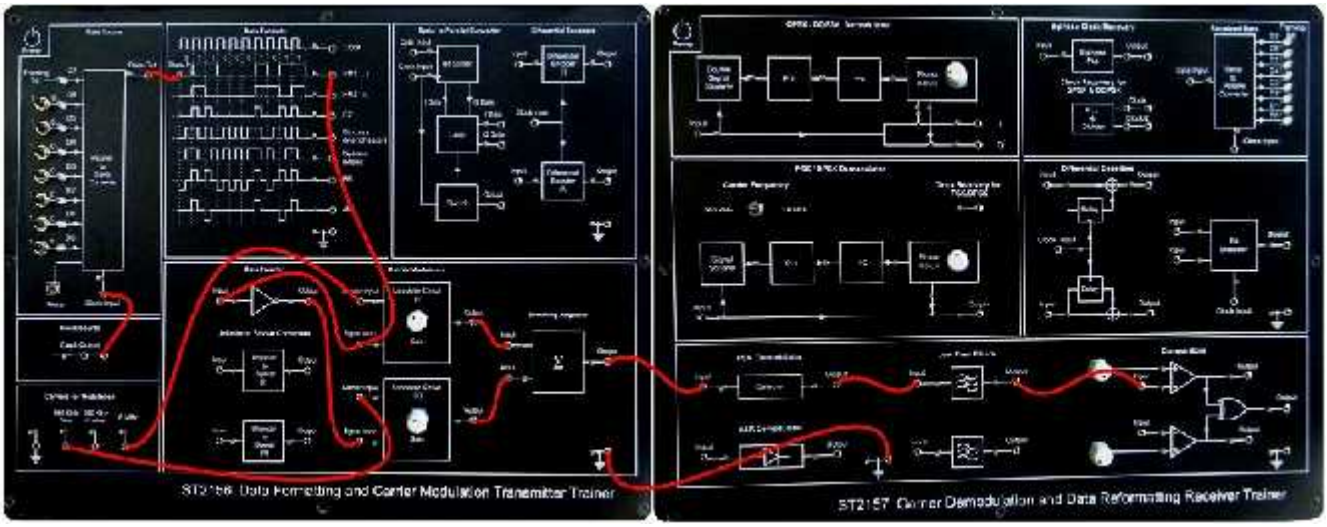


Fig.4.4

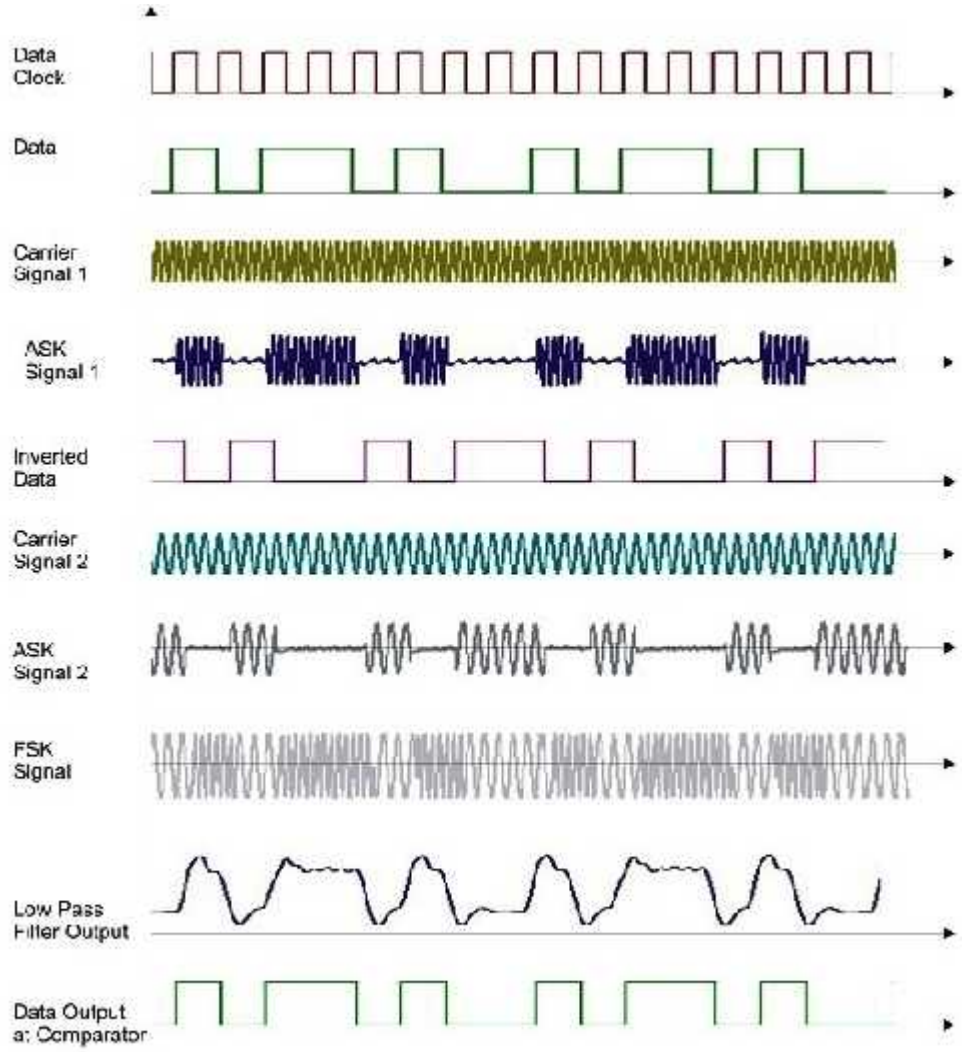
Procedure:

1. Connect the power supplies of ST2156 and ST2157 but do not turn on the power supplies until connections are made for this experiment.
2. Make the connections as shown in the figure 4.4.
    - Clock Source to Clock input of Data Source
    - Data out of Data Source to Data in of Data Formats
    - NRZ (L) to Signal input of Modular Circuit (I)
    - 1.6 MHz Carrier to Carrier input of Modular Circuit (I)
    - 900 KHz Carrier to Carrier input of Modular Circuit (II)
    - Data Inverter input to Signal input of Modular Circuit (I)
    - Data Inverter output to Signal input of Modular Circuit (II)
    - Output of Modular Circuit (I) to input of Summing Amplifier
    - Output of Modular Circuit (II) to input of Summing Amplifier
    - Output of Summing Amplifier to input of FSK Demodulator
    - Output of FSK Demodulator to input of Low Pass filter
    - Output of Low Pass filter to input of Comparator
    - Both Ground are connected
3. Switch 'ON' the power.

4. On ST2156, connect oscilloscope CH1 to 'Clock In' and CH2 to 'Data In' and observe the waveforms.
5. On ST2156, connect oscilloscope CH1 to 'NRZ (L)' and CH2 to 'Output' of Summing Amplifier on ST2156 and observe the waveforms.
6. Adjust the potentiometers of both the Modulator Circuit (I) & (II) onST2156 to adjust the amplitude of FSK waveform at Summing Amplifier's output on ST2156.
7. On ST2156, connect oscilloscope CH1 to 'NRZ (L)' and CH2 to 'Output' of comparator on ST2157 and observe the waveforms.

Observations:

1. The output at Summer Amplifier is the FSK waveform, Observe that for data bit '0' the FSK signal is at lower frequency (960KHz) & for data bit '1' the FSK signal is at higher frequency (1.6 MHz)The output at comparator on ST2157 is the same as 'Data In' on ST2156.



Waveforms of FSK Modulation & Demodulation

Fig 4.5

Conclusions:

1. The amplitude change in FSK waveform does not matter, therefore FSK modulation technique is very reliable even in noisy & fading channels.

Discussion:

Write briefly your comments about the above experiment.

SCIENTECH 2807

Apparatus Required:

- FSK Mod/DemodKit (**Scientech 2807**).
- A CRO / DSO

FSK Modulation:

Block Diagram:

FSK Modulator:

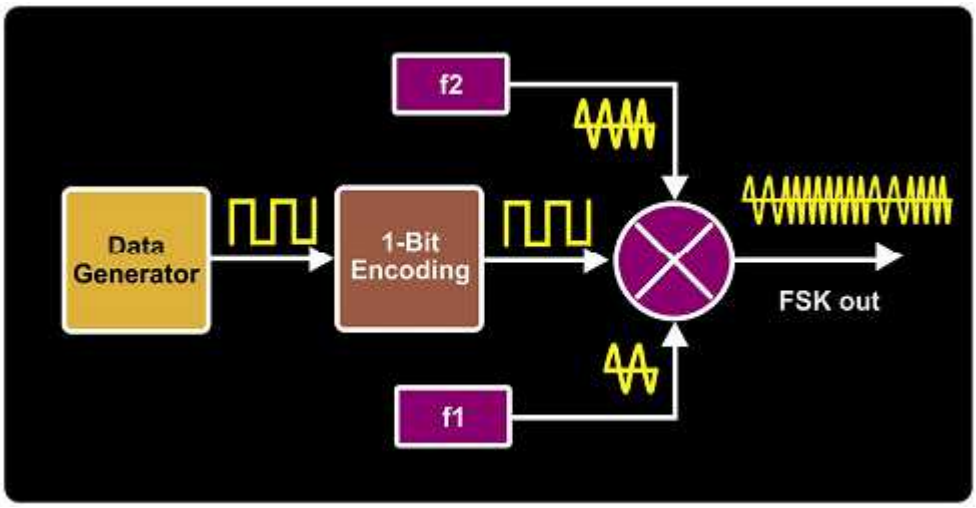


Fig. 4.6

Procedure:

2. Connect and switch on the power supply of Scientech 2807.
3. Select FSK modulator by *Modulation technique selection* button. On selection FSK, LED on TP28 will glows.
4. Select input *Data pattern* using push button i.e. 8-Bit, 16-Bit, 32-Bit, 64-Bit. And respective LED will glow. Observe the input Data on test point (TP2).
5. Select input *data clock* using push button i.e. 2 KHz, 4 KHz, 8 KHz, 16 KHz. Observe the change in frequency on test point (TP1).
6. Observe the change in carrier signal frequency ($f1$) on test point (TP30).

7. Observe the change in carrier signal frequency ($f2$) on test point (TP29), which twice then frequency $f1$.
8. Observe the encoded input data pattern at test point (TP28).
9. Observe the FSK modulated output at test point (TP31)

Observation:

1. Observe the input data clock at TP1.
2. Observe the input data at TP2.
3. Observe the encoded input data at TP28.
4. Observe the carrier signal at TP29.
5. Observe the carrier signal at TP30.
6. Observe the FSK modulated output at TP31
7. Observe the following data Patterns on TP2
   - 8-Bit: "10110010"
   - 16-Bit: "0100110110110010"
   - 32-Bit: "00000101000101111100101000111111"
   - 32-Bit: "10101100111000111110000111111000001111100001110001100101010001111010"

Demodulation:

FSK Demodulator:

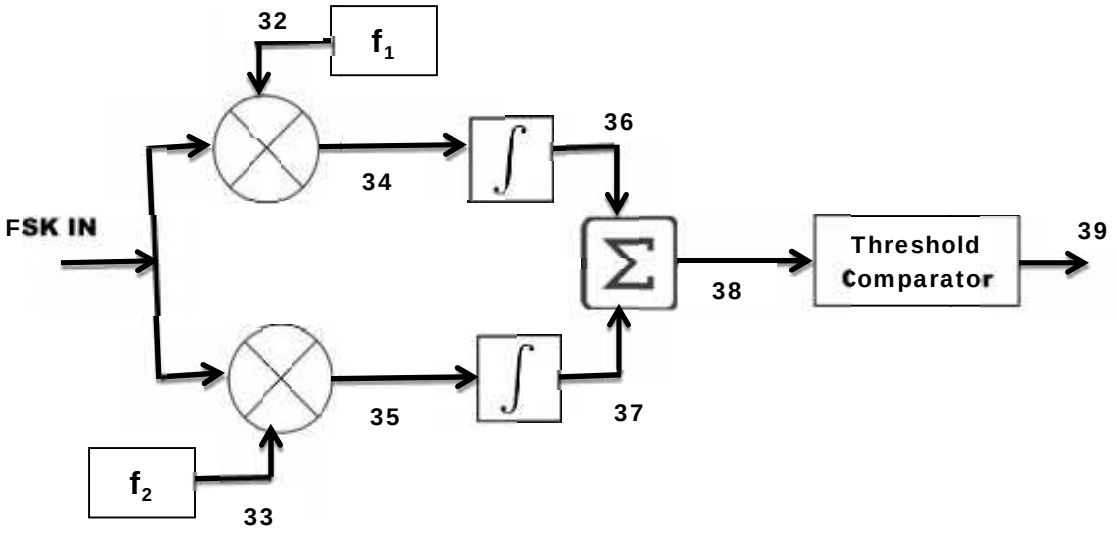


Fig. 4.7

At receiver side FSK modulated signal is multiplied by the carrier signals having frequencies f_1 and f_2. The output of multiplier consist of higher frequency and lower frequency components. This output then integrated by Integrator block. Summation of 1st Integrated output and 2nd Integrated output is performed in summer. This output is then passed from comparator block. Comparator block recovers digital data by comparing threshold value with integrated signal.

Procedure:

1. Connect and switch on the power supply of Scientech 2807.
2. Select FSK modulator by *Modulation technique selection* button. On selection FSK , LED on TP28 will glows.
3. Select input *Data pattern* using push button i.e. 8-Bit, 16-Bit, 32-Bit, 64-Bit. And respective LED will glow. Observe the input Data on test point (TP2).
4. Select input *data clock* using push button i.e. 2 KHz, 4 KHz, 8 KHz, 16 KHz. Observe the change in frequency on test point (TP1).
5. Observe the change in carrier signal frequency ($f1$) on test point (TP30) .
6. Observe the change in carrier signal frequency ($f2$) on test point (TP29), which twice then frequency $f1$.
7. Observe the encoded input data pattern at test point (TP28).
8. Observe the FSK modulated output at test point (TP31)
9. Observe the complex multiplier output at test point (TP34) and test point (TP35)
10. Observe the Integrator output at test point (TP36) and test point (TP37)
11. Observe the sigma (S) output at test point (TP38)
12. Observe FSK Demodulated output at test point (TP39)

Observation:

1. Observe the input data clock at TP1.
2. Observe the input data at TP2.
3. Observe the encoded input data at TP28.
4. Observe the carrier signal at TP29 and TP30.
5. Observe the FSK modulated output at TP31
6. Observe the complex multiplier output at TP34 and TP35
7. Observe the Integrator output at TP36 and TP37
8. Observe the sigma (S) output at TP38
9. Observe Demodulated output at TP39
10. Observe the following data Patterns on TP2
    - 8-Bit: "10110010"
    - 16-Bit: "0100110110110010"
    - 32-Bit: "00000101000101111100101000111111"
    - 32-Bit: "10101100111000111110000111111000001111100001110001100101010001111010"

Discussion:

Write briefly your comments about the above experiment.

Precautionary Measure to be taken:

1. Ensure that equipment or training kit switch is kept off. While connecting it to main power supply.

2. For connecting any signal from one equipment to another equipment or from one section to other section of the same kit, ensure that signal is grounded properly and subsequently connect the signal-to-signal line.
3. Handle gently all the necessary button or knob in the equipment avoiding all other buttons or knobs which are not required to be adjusted for the equipment.
4. For unusual spark or burning smell, immediately switch off the main supply to the kit.
5. Ensure that, a signal is connected to an appropriate junction destined for it.
6. Always cover the equipment for dust protection after the experiment.

Some Sample questions:

1. What is Frequency shift keying (FSK)?
2. Implement a system to transmit and receive a binary stream using FSK scheme and trace the waveforms.

EXPERIMENT # 5

Title: STUDY OF PHASE SHIFT KEYING (PSK)/ BINARY PHASE SHIFT KEYING (BPSK)

Objective:

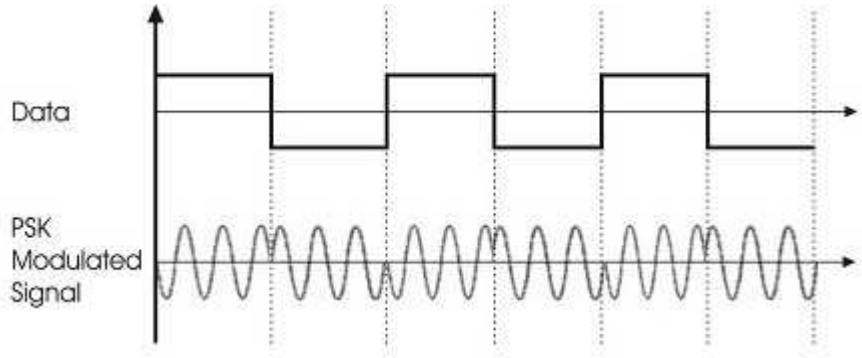
- Study of PSK/BPSK modulator and demodulator.

Theory:

Phase Shift Keying (PSK) is the digital modulation technique in which the phase of the carrier signal is changed by varying the sine and cosine inputs at a particular time. Phase shift keying involves the phase change of the carrier wave between 0° and 180° in accordance with the data levels to be transmitted. Phase shift keying is also known as phase reversal keying (PRK). The PSK waveform for a given data is as shown in figure 5.1.

In a simple PSK (i.e., binary PSK)

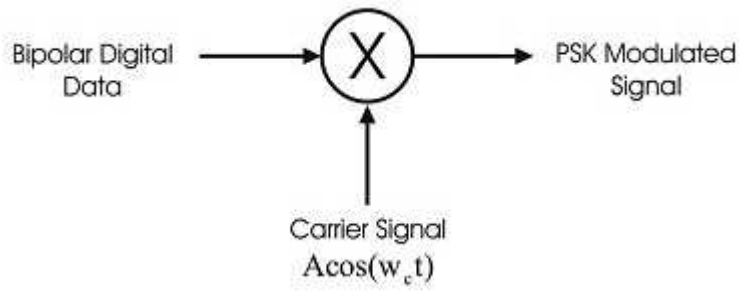
$S_0(t) = A\cos(\omega t)$ represents binary '0'
$S_0(t) = A\cos(\omega t + \pi)$ represents binary '1'



Phase Shift Keying Waveform

Fig. 5.1

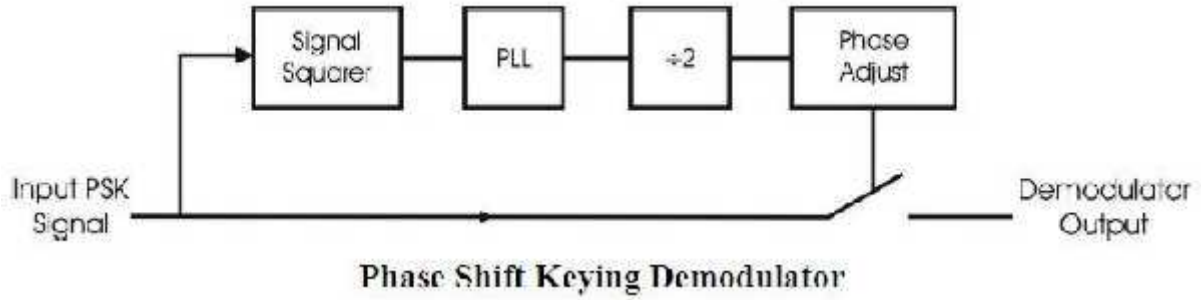
Functionally,PSK modulator usesbalanced modulator to multiply the carrier with the modulating signal. The digital signal applied to the modulation input for PSKgeneration is bipolar i.e. have equal positive and negative voltage levels. When themodulating input is positive the output ofmodulator is a sine wave in phase with thecarrier input. Whereas for the negative voltage levels, the output of modulator is asine wave which is shifted out of phase by 180° from the carrier input. This happensbecause the carrier input is now multiplied by the negative constant level.Thefunctional block representation of the PSK modulator is shown in the figure 5.2.



Phase Shift Keying Modulator

Fig. 5.2

In ST 2157, the square loop detector circuit is used for PSK signal demodulation. The PSKdemodulator is as shown in figure 5.3.



Phase Shift Keying Demodulator

Fig. 5.3

The incoming PSK signal with 0° & 180° phase changes is first fed to the signal squarer, which multiplies the input signal by itself. The output of this block is a signal of having twice the frequency to that of the input carrier frequency. As the frequency of the output doubled, the 0° & 180° phase changes are reflect as 0° & 360° phase changes. Since phase change of 360° is same as 0° phase change, it can be said that the signal squarer simply removes the phase transitions from the original PSK waveform.

The PLL block locks to the frequency of the signal square output & produces a clean square wave output of same frequency. To derive the square wave of same frequency as the incoming PSK signal, the PLL output is divided by two.

The following phase adjust circuit allows the phase of the digital signal to be adjusted with respect to the input PSK signal. Also its output controls the closing of an analog switch. When the output is high the switch closes & the original PSK signal is switched through the detector. When the output of phases adjust block is low, the switch opens & the output of detector output falls to 0 Volts. The demodulator output contains positive half cycles when the PSK input has one phase & only negative half cycles when the PSK input has another phase. The phase adjust potentiometer is adjusted properly. The average level information of the demodulator output which contains the digital data information is extracted by the following low pass filter. The low pass filter output is too rounded to be used for digital processing. Therefore it is 'Squared Up' by a voltage comparator.

ST2156 & ST2157

Apparatus Required:

- PSK Mod/DemodKit (ST2156 & ST2157).
- A CRO / DSO

Block/Connection Diagram:

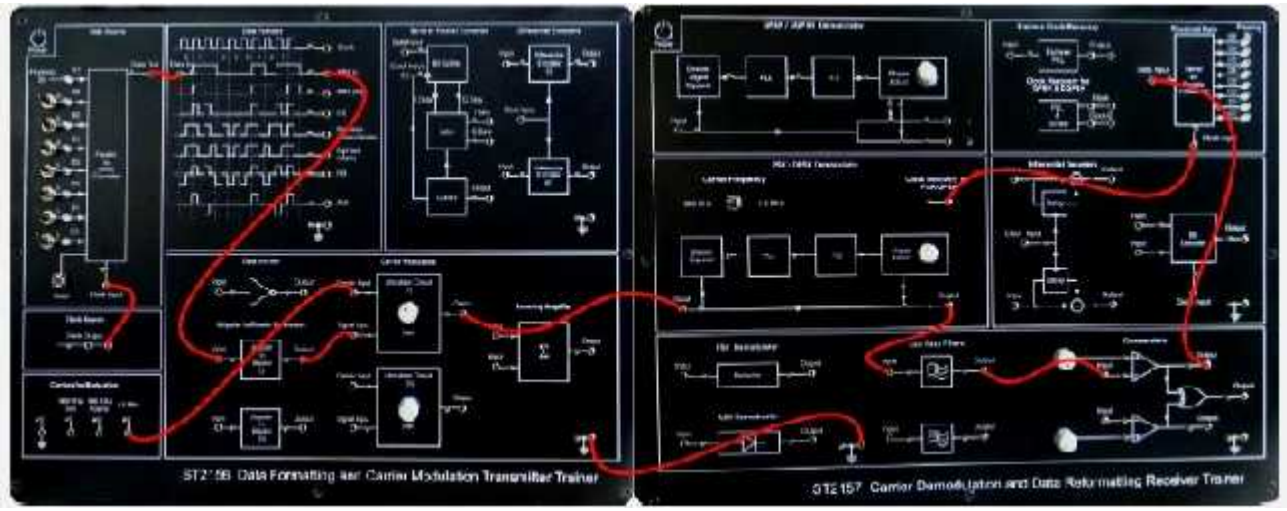


Fig. 5.4

Procedure:

1. Connect the power supplies of ST2156 and ST2157 but do not turn on the power supplies until connections are made for this experiment.
2. Make the connections as shown in the figure 5.4.
    - Clock Source to Clock input of Data Source
    - Data out of Data Source to Data in of Data Formats
    - NRZ (L) to input of Unipolar to Bipolar (I)
    - Output of Unipolar to Bipolar (I) to Signal input of Modular Circuit (I)
    - 1.6 MHz Carrier to Carrier input of Modular Circuit (I)
    - Output of Modular Circuit (I) to Input of PSK/DPSK Demodulator in ST2157
    - Output of PSK/DPSK Demodulator to Input of Low Pass filter
    - Output of Low Pass filter to input of Comparator
    - Output of Comparator to Data input of Serial to Parallel Converter
    - Clock Recovery for PSK/DPSK to Clock Input of Serial to Parallel Converter
    - Both Grounds are connected
3. Switch 'ON' the power.
4. On ST2156, connect oscilloscope CH1 to ‘Clock In’ and CH2 to ‘Data In’ and observe the waveforms.
5. On ST2156, connect oscilloscope CH1 to ‘NRZ (L)’ and CH2 to ‘Output’ of Modulator Circuit (I) on ST2156 and observe the waveforms.

6. Adjust the 'Gain' potentiometer of the Modulator Circuit (I) on ST2156 to adjust the amplitude of PSK waveform at output of Modulator Circuit (I) on ST2156.
7. Now on ST2157 connect oscilloscope CH1 to 'Input' of PSK demodulator and connect CH2 one by one to output of double squaring circuit, output of PLL, output of Divide by four (÷ 2) observe the wave forms.
8. On ST2157 connect oscilloscope CH1 to output of Phase adjust and CH2 to 'output' of PSK demodulator and observe the waveforms. Set all toggle switch to 0 and compare the waveform now vary the phase adjust potentiometer and observe its effects on the demodulated signal waveform. (Note: If there is problem in setting the waveform with potentiometer then toggle the switch given in PSK demodulator block two to three times to get the required waveform).
9. Now connect oscilloscope CH1 to 'PSK' output of PSK demodulator on ST2157 and connect CH2 'Output' of Low Pass Filter on ST2157 and observe the waveforms.
10. Connect oscilloscope CH1 to 'Output' of Low Pass Filter on ST2157 then connect CH2 to 'Output' of Comparator on ST2157 and observe the waveforms, now vary the reference voltage potentiometer of first comparator to generate desired data pattern.
11. On ST2156, connect oscilloscope CH1 to 'NRZ (L)' and CH2 to 'Output' of comparator on ST2157 and observe the waveforms.
12. Connect oscilloscope CH1 to 'Data In' then connect CH2 output to Bit decoder and observe the waveforms. If both data does not matches then try to match it by varying the phase adjust potentiometer on QPSK Demodulator.
13. Now try to match the LED sequence by once pressing the reset switch on ST2156.

Observations:

1. The output at 'Data In' is repeating sequence of bits generated by Data Source.
2. The 'Output' of Modulator Circuit (I) is Phase Shift Keying modulated signal.
3. The output of Double squaring circuit is sinusoidal signal (carrier signal) but frequency is four times higher than that of carrier used for modulation.
4. The output of Phase Lock Loop (PLL) is clock signal of same frequency as that of the output of double squaring circuit and output of Divide by two (÷ 2) is clock signal of frequency two times less than the output of PLL signal.
5. The output of PSK demodulator is a signal having group of positive half cycles and group of negative half cycles of the carrier signal.
6. A low pass filter removes high frequency component from demodulated PSK signal and it makes the signal smooth.
7. The variation in reference voltage potentiometer affect the Data, to recover Data correctly potentiometer adjustment is necessary.
8. The Phase Adjust potentiometer on ST2157 matches the phase of regenerated clock and carrier with input clock and carrier signal.

Waveforms of PSK Modulation:

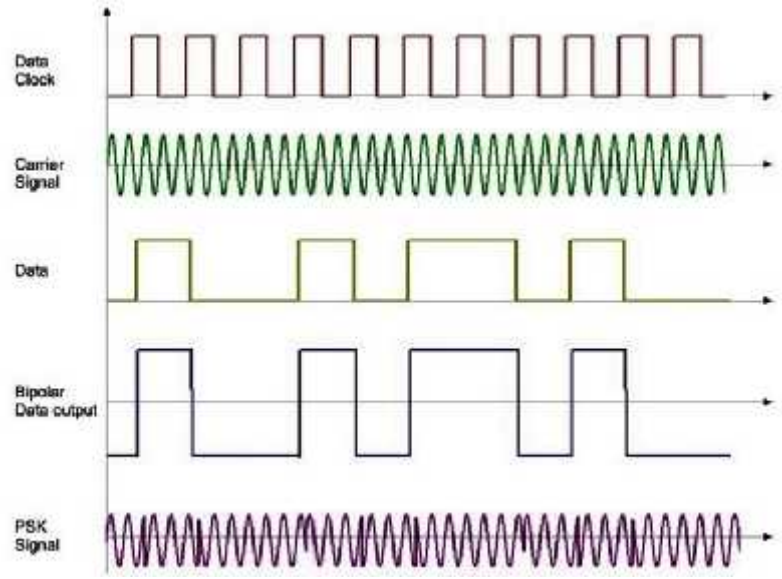


Fig 5.5

Waveforms of PSK Demodulation:

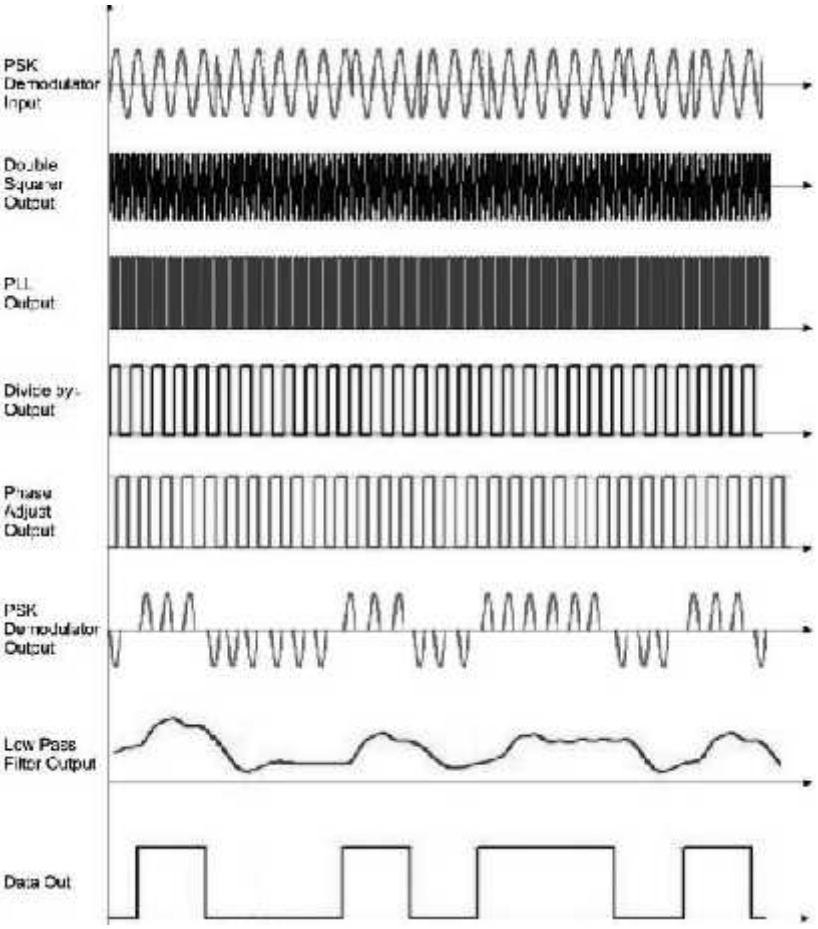


Fig 5.6

Conclusions:

1. The Binary Phase Shift Keying modulation is correct for different Data pattern and also correct for clock and carrier frequencies.

Discussion:

Write briefly your comments about the above experiment.

SCIENTECH 2807

Apparatus Required:

- BPSK Mod/DemodKit (**Scientech 2807**).
- A CRO / DSO

BPSK Modulation:

Block Diagram:

BPSK Modulator:

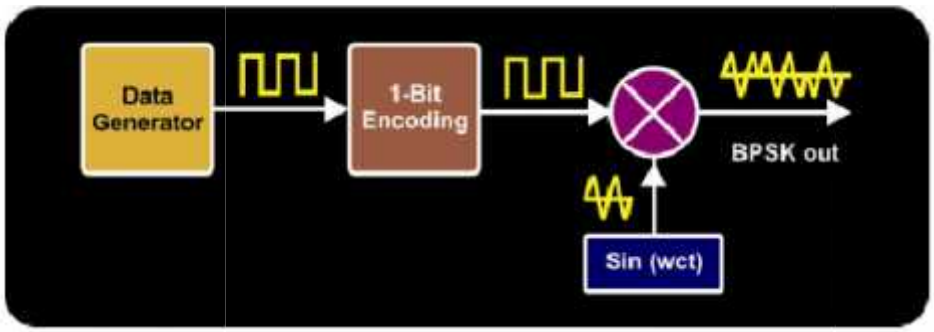


Fig. 5.7

Procedure:

2. Connect and switch on the power supply of Scientech 2807.
3. Select Binary PSK modulator by *Modulation technique selection* button. On selection Binary PSK LED on TP10 will glows.
4. Select input *Data pattern* using push button i.e. 8-Bit, 16-Bit, 32-Bit, 64-Bit. And respective LED will glow. Observe the input Data on test point (TP2).

5. Select input *data clock* using push button i.e. 2 KHz, 4 KHz, 8 KHz, 16 KHz. Observe the change in frequency on test point (TP1).
6. Observe the change in carrier signal frequency on test point (TP11).
7. Observe the encoded input data pattern at test point (TP10).
8. Observe the BPSK modulated output at test point (TP12)

Observation:

1. Observe the input data clock at TP1.
2. Observe the input data at TP2.
3. Observe the encoded input data at TP10.
4. Observe the carrier signal at TP11.
5. Observe the BPSK modulated output at TP12
6. Observe the following data Patterns on TP2
   - 8-Bit: "10110010"
   - 16-Bit: "0100110110110010"
   - 32-Bit: "00000101000101111100101000111111"
   - 32-Bit: "10101100111000111110000111111000000111110000111000110010101000111010"

BPSK Demodulation:

The incoming modulated BPSK signal is multiplied with the carrier signal generated from the carrier generator. The output of the multiplier contains high ($f_{in}+f_{nco}$) and low ($f_{in}- f_{nco}$) frequency components. The integrator block integrates multiplier output. With the help of comparator by comparing thresh hold value input data is received.

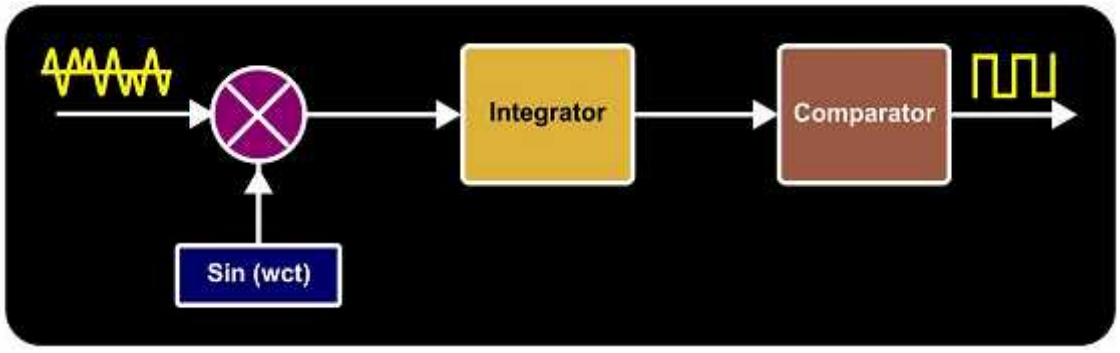


Fig. 5.8

Procedure:

1. Connect and switch on the power supply of Scientech 2807.

2. Select Binary PSK modulator using *Modulation technique selection* button. On selection of Binary PSK technique LED on TP10 will glows.
3. Select input *Data pattern* using push button i.e. 8-Bit, 16-Bit, 32-Bit, 64-Bit And respective LED will glow. Observe the input Data on test point (TP2).
4. Select input *data clock* using push button i.e. 2 KHz, 4 KHz, 8 KHz, 16 KHz. Observe the change in frequency on test point (TP1).
5. Observe the change in carrier signal frequency on test point (TP11) & test point (TP13).
6. Observe the encoded data pattern at test point (TP10).
7. Observe the BPSK modulated output at test point (TP12)
8. Observe the complex multiplier output at test point (TP14)
9. Observe the Integrator output at test point (TP15)
10. Observe Demodulated output at test point (TP16)

Observation:

1. Observe the Input Data at TP2 .
2. Observe the Input data clock at TP1.
3. Observe the 1-bit encoded input data at TP10.
4. Observe the Carrier signal at TP11 and TP13.
5. Observe the Modulated output at TP12.
6. Observe the multiplier output at TP14
7. Observe the Integrator output at TP15
8. Observe the Demodulated output at TP16
9. Observe the following data Patterns on TP2
   - 8-Bit: "10110010"
   - 16-Bit: "0100110110110010"
   - 32-Bit: "00000101000101111100101000111111"
   - 32-Bit: "10101100111000111100001111100000111100001110001100101010001111010"

Discussion:

Write briefly your comments about the above experiment.

Precautionary Measure to be taken:

1. Ensure that equipment or training kit switch is kept off. While connecting it to main power supply.
2. For connecting any signal from one equipment to another equipment or from one section to other section of the same kit, ensure that signal is grounded properly and subsequently connect the signal-to-signal line.
3. Handle gently all the necessary button or knob in the equipment avoiding all other buttons or knobs which are not required to be adjusted for the equipment.
4. For unusual spark or burning smell, immediately switch off the main supply to the kit.
5. Ensure that, a signal is connected to an appropriate junction destined for it.
6. Always cover the equipment for dust protection after the experiment.

Some Sample questions:

1. What is BPSK signal? Why BPSK is used?
2. Implement a system to transmit and receive the data using BPSK modulation anddemodulation scheme and trace the waveforms. Measure the related frequencies.

EXPERIMENT # 6

Title: STUDY OF QUADRATUREPHASE SHIFT KEYING (QPSK)

Objective:

- Study of PSK/BPSK modulator and demodulator.

Theory:

QPSK is a form of phase modulation technique, in which two information bits (combined as one symbol) are modulated at once, selecting one of the four possible carrier phase shift states. Recall that in binary PSK (BPSK), the change in logic level causes the BPSK signal's phase to change, it does so by 180o.

It allows one symbol to transfer two bits of data. There are four possible two-bit numbers (00, 01, 10, 11), and consequently we need four phase offsets. Again, we want maximum separation between the phase options, which in this case is 90°
We have 360° of phase to work with and four phase states, and thus the separation should be 360°/4 = 90°. So our four QPSK phase shifts are 45°, 135°, 225°, and 315°.

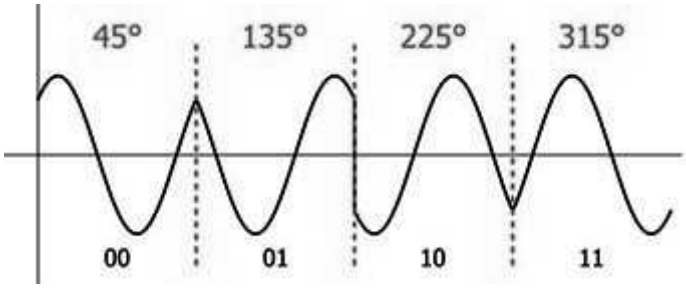


Fig. 6.1

The QPSK modulator can be configured as shown in the figure 6.2

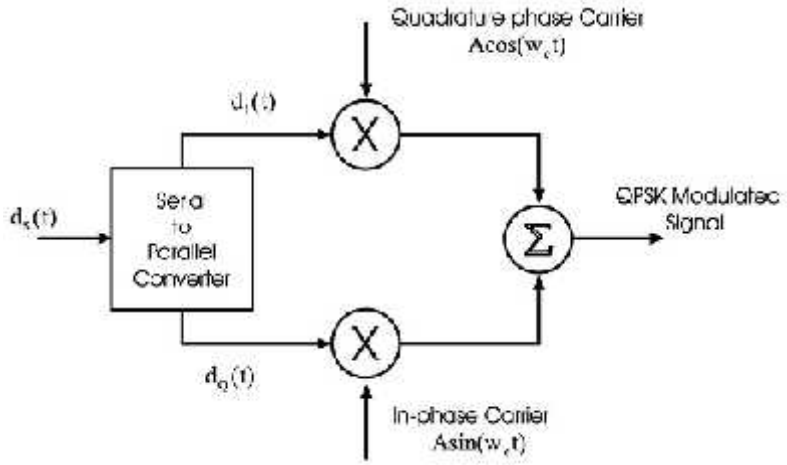


Fig. 6.2

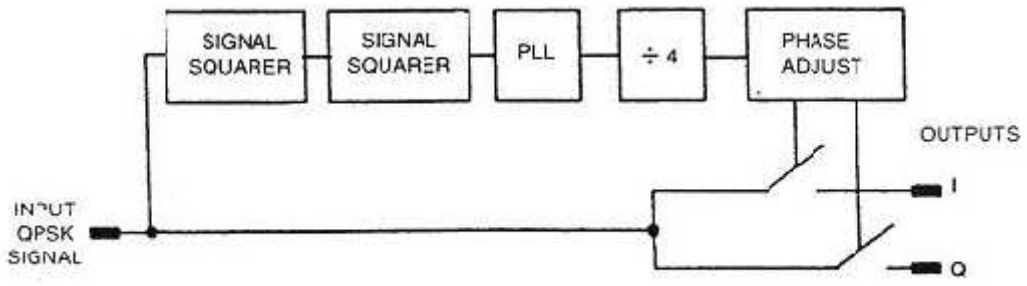
The two carriers namely I & Q as has been stated, have same frequency but differ in phase by 90°. Also the I data refer to the Dibit MSB & Q data refers to the Dibit LSB. Each modulator performs phase-shift keying on its respective carrier input in accordance with respective data input such that,

1. The output of modulator 1 is a PSK signal with phase shift of 0° and 180° respectively, relative to the I-carrier, and
2. The output of modulator 2 is a PSK signal with phase shift of 90° and 270°respectively, relative to the I-carrier.

The output of the two modulators is summed by a summing amplifier. The phase of the summing amplifier's output signal relative to I-carrier, at any instance of time takes one of the four phases 45° 135°,225°, and 315° depending on the applied Dibit code. When these Dibit codes alter, the phase of the QPSK output changes by 0°, 90°, 180° or 270° from its previous phase position. Thus the output of the summing amplifier is a QPSK waveform.

Quadrature Phase Shift Keying Demodulator:

The incoming QPSK signal is first squared in the signal squarer 1. The functioning of the signal squarer has already been discussed in the PSK Modulator section. The output of the signal squarer 1 is a signal at twice the original frequency with phase changes reduced to 0° & 180°. This is because all the phase changes are also doubled. The 0° & 180° phase changes becomes 0° (as 2 x 180° = 60° = 0° phase shift.) and the 90° and 270° phases both become 180° (since 270° + 270° = 540° = 180° phase shift)



Quadrature Phase Shift Keying Demodulator

Fig. 6.3

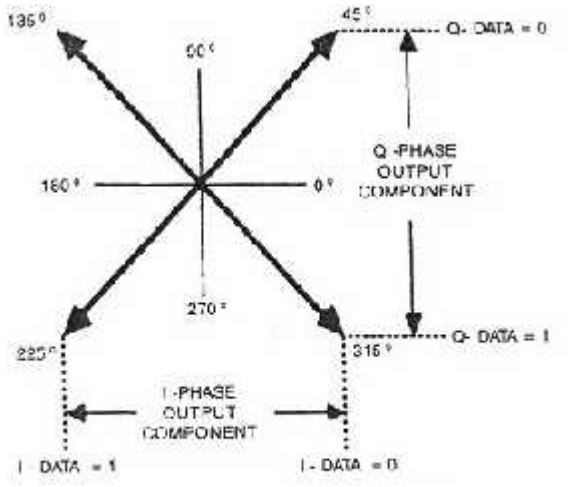
The output of the signal squarer 1 is fed to signal 1. The output of the signal squarer 1 is fed to signal squarer 2. This circuit is identical to signal squarer with frequency double that of the signal at its input (Quadrupled with respect to the original QPSK input signal frequency). The 0° and 180° phases changes are also reduced to a 0° phase changes are also reduced to 0° phases shift, since the phases are also doubled (Also 2 x 180° = 360° = 0° phase shift).

Therefore, the output from signal squarer 2 is a sinewave at four times the frequency of the original QPSK carrier signal with no phase changes.

The output of signal squarer 2 is fed to the phase locked loop (PLL) which locks on the incoming signal & produces a square wave of same frequency as that of the input. The output of PLL is divided in frequency by a factor of 4 by a ÷ 4 circuit. Now the frequency is same as that of the QPSK carrier signal.

The next stage in demodulation is a phase adjusts Circuit. The output of the phase adjust circuit are two square waves of same frequency as the input signal applied and with 90° phase shift

between them. Also the phase of the two output signals can also be adjusted relative to the original QPSK signal. Note that the 90° phase difference between the two outputs is maintained.
The output of the phase circuit controls the two analog switches. The switch is closed when thecorresponding output goes high. The original QPSK signal is then switchedthrough to one of the QPSK demodulator. How output can be input with a low level,the switches are open & the output is pulled down to 0V.
The two outputs from the demodulator are labeled I & Q. Once the correct phaserelation betweenQPSK signal & phase adjust output have been set, the I & Q outputswill contain information about original two bit code. This is illustrated in phase or diagram. See figure 6.4.

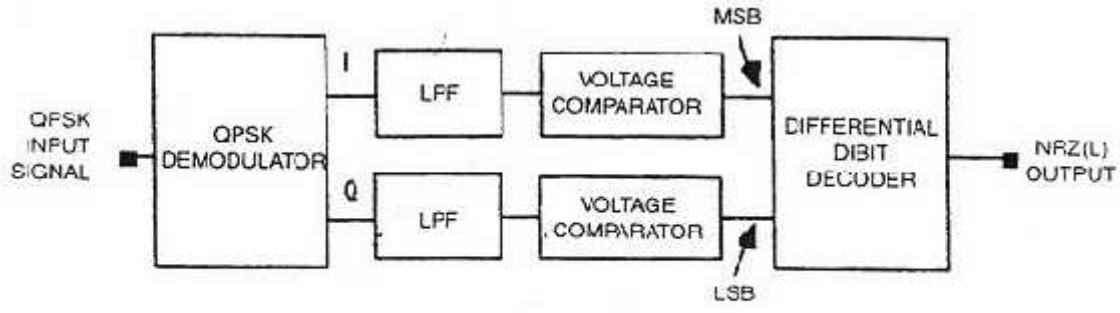


All Angles represent phase LAG with respect to 0°

Phasor Diagram

Fig.6.4

The average level of the I& Q outputs contains information about the Dibit code. The average level of the two outputs is extracted by passing them through the low pass filter. The output of the filters is rounded & cannot be used for digital processing. The wave 'Squared Up' by a voltage a comparator circuit. As shown in the figure 6.5.



Quadrature Phase Shift Keying Receiver

Fig. 6.5

ST2156 & ST2157

Apparatus Required:

- PSK Mod/DemodKit (ST2156 & ST2157).
- A CRO / DSO

Block/Connection Diagram:

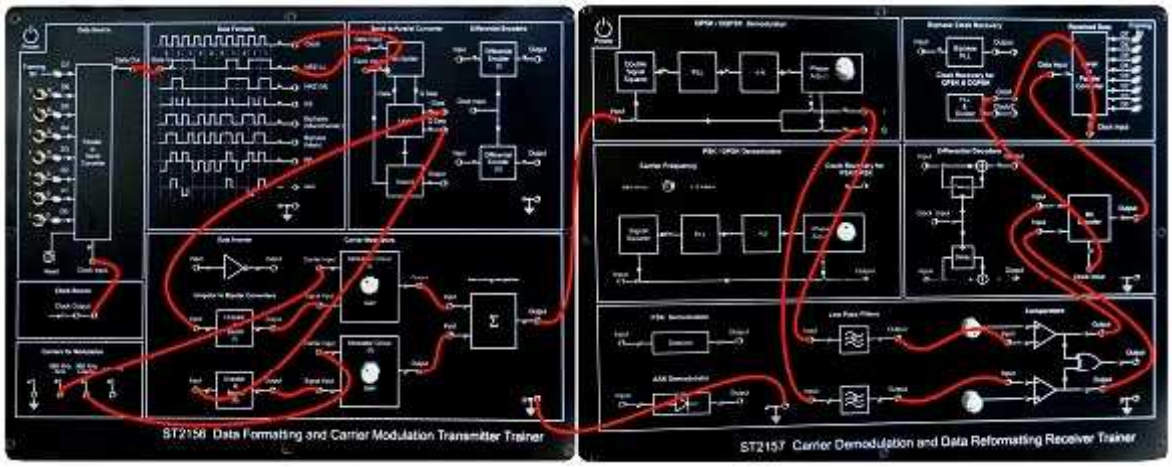


Fig. 6.6

Procedure:

1. Connect the power supplies of ST2156 and ST2157 but do not turn on the power supplies until connections are made for this experiment.
2. Make the connections as shown in the figure 6.6.
    - Clock Source to Clock input of Data Source.
    - Data out of Data Source to Data in of Data Formats.
    - NRZ (L) to Data input of Bit Splitter of Serial to Parallel Converter.
    - Clock of Data Formats to Clock input of Bit Splitter of Serial to Parallel Converter.
    - I Data of Latch of Serial to Parallel Converter to input of Unipolar to Bipolar (I).
    - Output of Unipolar to Bipolar (I) to Signal Input of Modular Circuit (I).
    - 900 KHz Sineto Carrier input of Modular Circuit (I).
    - Q Data of Latch of Serial to Parallel Converter to input of Unipolar to Bipolar (II).
    - Output of Unipolar to Bipolar (II) to Signal Input of Modular Circuit (II).
    - 900 KHz Cosine to Carrier input of Modular Circuit (II).
    - Output of Modular Circuit (I) to Input1 of Summing Amplifier.
    - Output of Modular Circuit (II) to Input 2 of Summing Amplifier.
    - Output of Summing Amplifier to Input of QPSK/DQPSK Demodulator in ST2157.
    - I of QPSK/DQPSK Demodulator Input of Low Pass filter1
    - Q of QPSK/DQPSK Demodulator Input of Low Pass filter 2

- Output of Low Pass filter1 to Input of Comparator1
- Output of Low Pass filter 2 to Input of Comparator2
- Output of Comparator1 to Input 1 of Bit Decoder.
- Output of Comparator2 to Input 2 of Bit Decoder.
- Output of Bit Decoder to Data Input of Serial to Parallel Converter in ST2157.
- Clock of PLL & Divider to Clock Input of Serial to Parallel Converter in ST2157
- Clock of PLL & Divider to Clock Input of Bit Decoder in ST2157.
- Both Grounds are connected

3. Switch 'ON' the power.
4. On ST2156, connect oscilloscope CH1 to 'Clock In' and CH2 to 'Data In' and observe the waveforms.
5. On ST2156, connect oscilloscope CH1 to 'Clock Output' and CH2 one by one to 'Sine' and 'Cosine' output of 960 KHz and observe the waveforms.
6. On ST2156, connect oscilloscope CH1 to 'Data In' and connect CH2 one by one to 'I Data' and 'Q Data' outputs and observe the waveforms.
7. Now connect oscilloscope CH1 to 'I Data' output on ST2156 and connect CH2 one by one to 'Signal In', 'Carrier In' and 'Output' of modulator circuit (I) on ST2156 and observe the waveforms.
8. Now connect oscilloscope CH1 to 'Q Data' output on ST2156 and connect CH2 one by one to 'Signal In', 'Carrier In' and 'Output' of modulator circuit (II) on ST2156 and observe the waveforms.
9. Now connect oscilloscope CH1 to 'Data Out' on ST2156 and CH2 to 'Output' of Summing Amplifier on ST2156 and observe the waveforms.
10. Set 'Carrier frequency' selection switch to '960 KHz' on ST2157.
11. Now on ST2157 connect oscilloscope CH1 to 'Input' of QPSK demodulator and connect CH2 one by one to output of double squaring circuit, output of PLL, output of Divide by four (÷ 4) observe the wave forms.
12. On ST2157, connect oscilloscope CH1 to 'I' output of QPSK demodulator and CH2 to 'Q' output of QPSK demodulator and observe the waveforms. Set all toggle switch to 0, now vary the phase adjust potentiometer and observe its effects on the demodulated signal waveforms.
13. Connect oscilloscope CH1 to 'I' output of QPSK demodulator on ST2157 then connect CH2 one by one to output of low pass filter, output of Comparator on ST2157 and observe the waveforms.
14. Connect oscilloscope CH1 to 'Q' output of QPSK demodulator on ST2157 then connect CH2 one by one to output of low pass filter, output of Comparator on ST2157 and observe the waveforms.
15. Compare the output of comparators on ST2157 with the output 'I Data' and 'Q Data' on ST2156 respectively.
16. Connect oscilloscope CH1 to 'Data In' then connect CH2 output to Bit decoder and observe the waveforms. If both data does not matches then try to match it by varying the phase adjust potentiometer on QPSK Demodulator.
17. Now try to match the LED sequence by once pressing the reset switch on ST2156.

Observations:

1. The output at 'Data In' is repeating sequence of bits generated by Data Source.
2. The 'I Data' and 'Q Data' output are even and odd bit sequence of input data sequence and bit duration is double of input data sequence as shown in the figure 6.7.
3. The 'Output' of Modulator Circuit (I) and Modulator Circuit (II) are Phase Shift Keying modulated signals, and summation of these two signals are Quadrature Phase Shifted signal as shown in the figure 6.7.
4. The output of Double squaring circuit is sinusoidal signal (carrier signal) butfrequency is four times higher than that of carrier used.
5. The output of Phase Lock Loop (PLL) is clock signal of same frequency as thatof the output of double squaring circuit and output of Divide by four (÷ 4) isclock signal of frequency four times less than the output of PLL signal.
6. The output of QPSK demodulator is a signal having group of positive halfcycles and group of negative half cycles of the carrier signal as shown in thefigure 6.8.
7. A low pass filter removes high frequency component from demodulated QPSK signal and it makes the signal smooth as shown in the figure 6.8.
8. The variation in reference voltage potentiometer affect the Data, to recover Data correctly potentiometer adjustment is necessary and recovered Data.

Waveforms of QPSK Modulation:

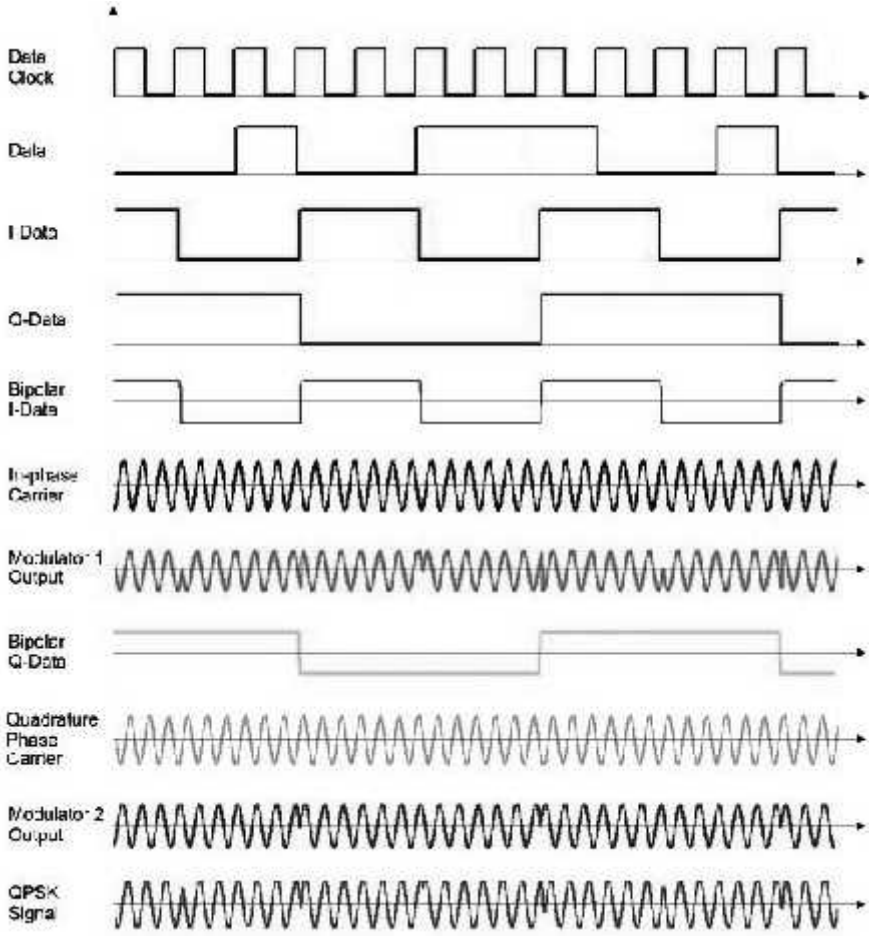


Fig. 6.7

Waveforms of PSK Demodulation:

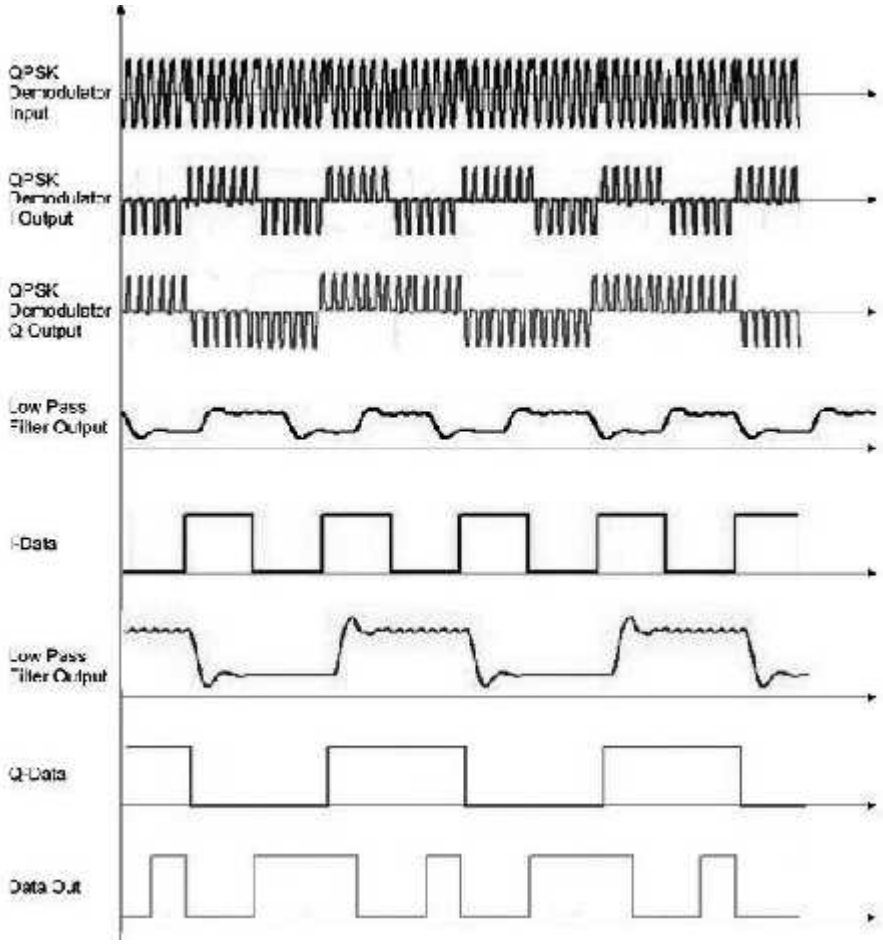


Fig. 6.8

Conclusions:

1. The Quadrature Phase Shift Keying modulation is correct for different Data pattern and also correct for clock and carrier frequencies.

Discussion:

Write briefly your comments about the above experiment.

SCIENTECH 2808

Apparatus Required:

- QPSK Mod/DemodKit (**Scientech 2808**).
- A CRO / DSO

QPSK Modulation:

Block Diagram:

BPSK Modulator:

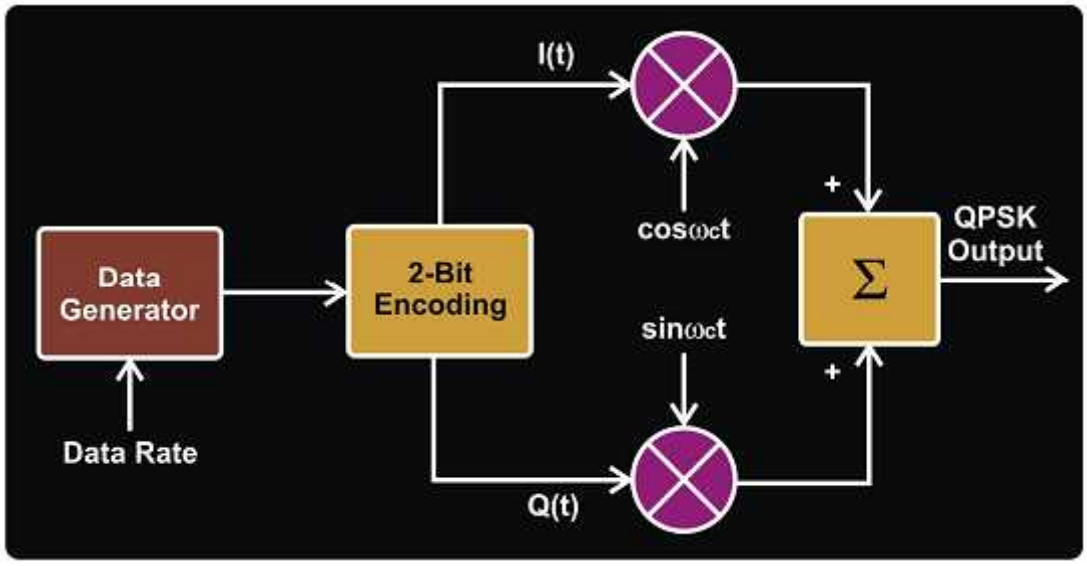


Fig. 6.9

Procedure:

1. Connect and switch on the Power Supply of Scientech 2808
2. Quadrature Phase Shift Keying Modulator is selected by default and LEDs of corresponding technique will glow when user switch on the power.
3. Select *bit pattern* using push button i.e. 8 bit, 16 bit, 32 bit and 64 bit. And respective LED will glow. Observe the bit pattern on test point (TP2).
4. Select *data rate* using push button i.e. 2 KHz, 4 KHz, 8 KHz and 16 KHz. Observe the change in frequency on test point (TP1).

Observation:

1. Observe the input bit pattern at TP2 by varying bit pattern using respective push button.
2. Observe the data rate at TP1 by varying data rate using push button.
3. Observe the 2-bit encoding i.e., I-Channel (TP3) and Q-Channel (TP4).
4. Observe Carrier Signal i.e., Sine (TP6) and Cosine (TP5), Frequency of Carrier signal will change w.r.t data rate.
5. Observe I-Channel (TP7) and Q-Channel (TP8) Modulated Signal.
6. Observe QPSK Modulated Signal at TP9.

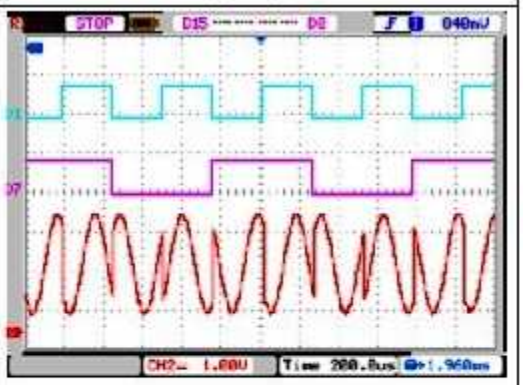
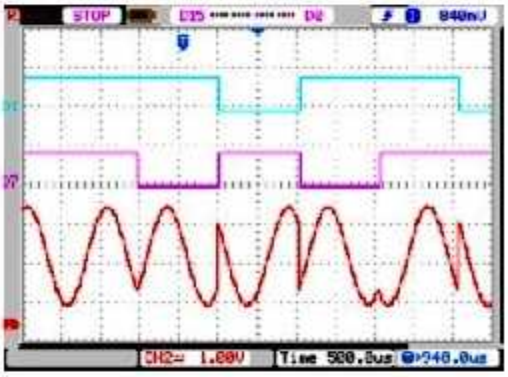
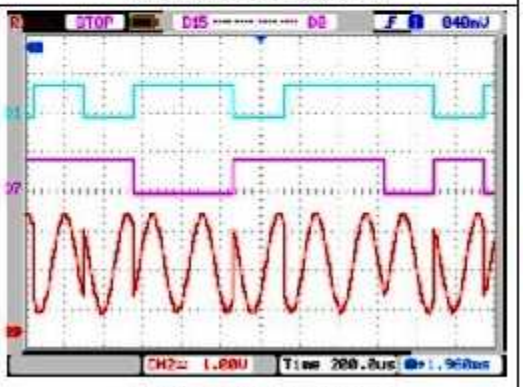
Data Bit	Data Rate	DSO Results
8 Bit	16 KHz	 D1:TP3 D7:TP4 CH2:TP9
32 Bit	4 KHz	 D1:TP3 D7:TP4 CH2:TP9
32 Bit	16 KHz	 D1:TP3 D7:TP4 CH2:TP9

Fig. 6.10

QPSK Demodulation:

The incoming modulated BPSK signal is multiplied with the carrier signal generated from the carrier generator. The output of the multiplier contains high ($f_{in}+f_{nco}$) and low ($f_{in}- f_{nco}$) frequency components. The integrator block integrates multiplier output. With the help of comparator by comparing thresh hold value input data is received.

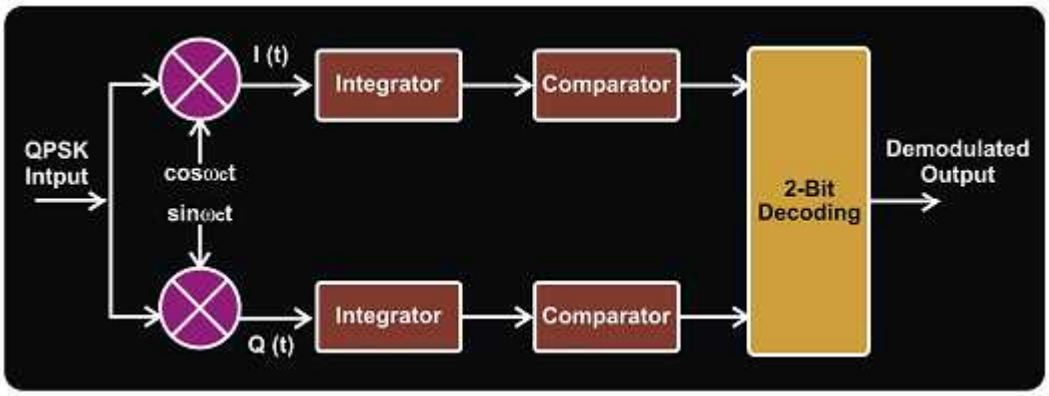


Fig. 6.11

Procedure:

1. Connect and switch on the Power Supply of Scientech 2808
2. Quadrature Phase Shift Keying Modulator is selected by default and LEDs of corresponding technique will glow when user switch on the power.
3. Select *bit pattern* using push button i.e. 8 bit, 16 bit, 32 bit and 64 bit. And respective LED will glow. Observe the bit pattern on test point (TP2).
4. Select *data rate* using push button i.e. 2 KHz, 4KHz, 8 KHz and 16 KHz. Observe the change in frequency on test point (TP1).

Observation:

1. Observe the input bit pattern at TP2 by varying bit pattern using respective push button.
2. Observe the data rate at TP1 by varying data rate using push button.
3. Observe the 2-bit encoding i.e., I-Channel (TP3) and Q-Channel (TP4).
4. Observe Carrier Signal i.e., Sine (TP6) and Cosine (TP5), Frequency of Carrier signal will change w.r.t data rate.
5. Observe I-Channel (TP7) and Q-Channel (TP8) Modulated Signal.
6. Observe QPSK Modulated Signal at TP9.
7. Observe the multiplied Signal of QPSK and Carrier signal Cosine at TP12 & QPSK and carrier signal Sine at TP13.
8. Observe the integrated output of I-Channel TP14 and Q-Channel TP15.
9. Observe the comparator output of I-Channel TP16 and Q-Channel TP17 that is same as at input with delay.
10. Observe the QPSK Demodulated Signal at TP18.

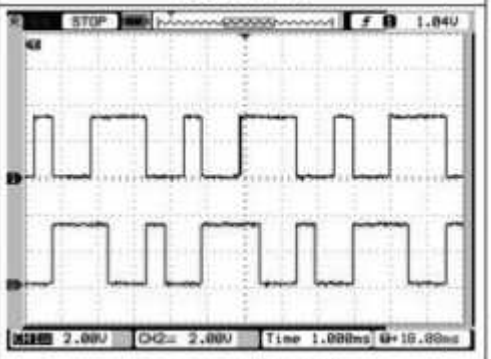
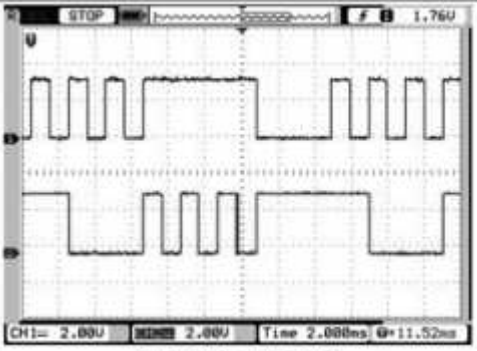
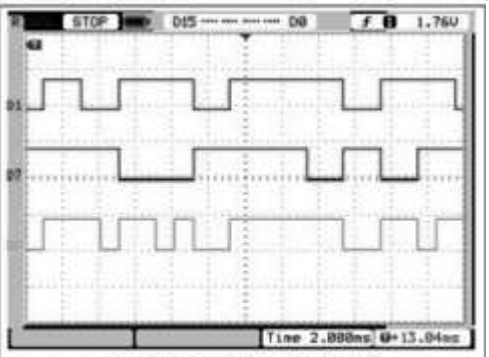
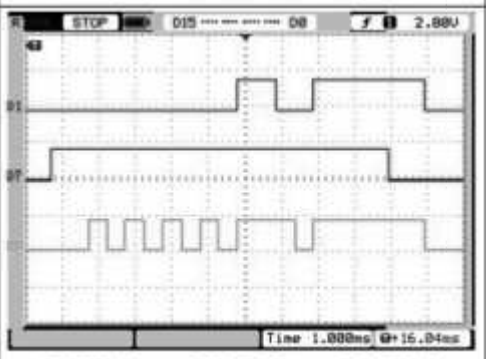
Data Bit	Data Rate	DSO Results
8 Bit	4 KHz	 CH1: TP2 CH2: TP18
16 Bit	2 KHz	 CH1: TP2 CH2: TP18
32 Bit	2 KHz	 D1: TP16 D7: TP17 D10:18
64 Bit	4 KHz	 D1: TP16 D7: TP17 D10:TP18

Fig. 6.12

Discussion:

Write briefly your comments about the above experiment.

Precautionary Measure to be taken:

1. Ensure that equipment or training kit switch is kept off. While connecting it to main power supply.
2. For connecting any signal from one equipment to another equipment or from one section to other section of the same kit, ensure that signal is grounded properly and subsequently connect the signal-to-signal line.
3. Handle gently all the necessary button or knob in the equipment avoiding all other buttons or knobs which are not required to be adjusted for the equipment.
4. For unusual spark or burning smell, immediately switch off the main supply to the kit.
5. Ensure that, a signal is connected to an appropriate junction destined for it.
6. Always cover the equipment for dust protection after the experiment.

Some Sample questions:

1. What is Quadrature Phase Shift Keying Modulator and how it works?
2. Implement a system to transmit and receive the data using QPSK modulation anddemodulation scheme and trace the waveforms. Measure the related frequencies.

EXPERIMENT # 7

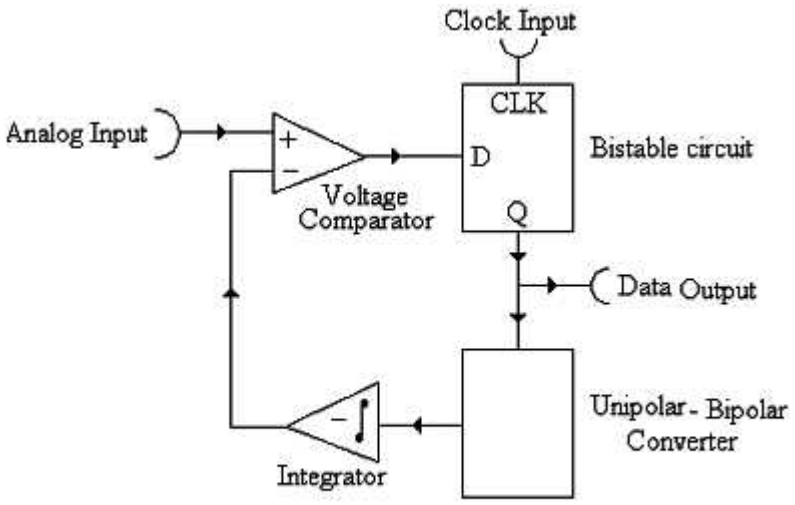
Title: STUDY OF DELTA MODULATION AND DEMODULATION TECHNIQUES

Objective:

- Study of Deltamodulator and demodulator.

Theory:

Delta modulation (DM or Δ-modulation) is an analog-to-digital and digital-to-analog signal conversion technique used for transmission of voice information where quality is not of primary importance. DM is the simplest form of differential pulse-code modulation (DPCM) where the difference between successive samples is encoded into n-bit data streams. In delta modulation, the transmitted data is reduced to a 1-bit data stream.Figure 7.1 shows the block diagram of delta modulator



Delta modulator

Fig. 7.1

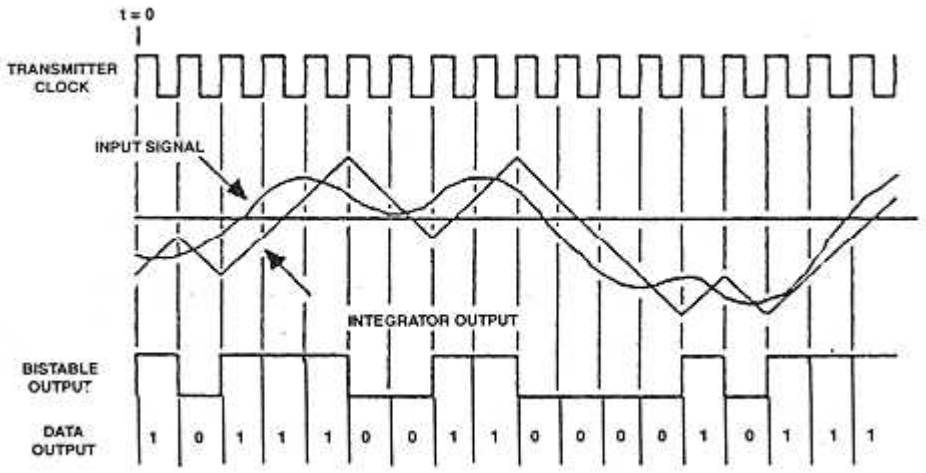
The analog signal which is to be encoded into digital data is applied to the +ve input of the voltage comparator which compares it with the signal applied to its -ve input from the integrator output.
The comparator's output is logic '0' or '1' depending on whether the input signal at +ve terminal is lower or greater than the -ve terminals input signal.
The comparator's output is then latched into a D-flip-flop which is clocked by the transmitter clock. Thus, the output of D-flip-Flop is a latched 'l' or '0' & synchronized with the transmitter clock edge.
This binary data stream is transmitted to receiver and is also fed to the unipolar to bipolar converter. This block converts logic '0' to voltage level of + 4V and logic 'l' to voltage level - 4V.
The Bipolar output is applied to the integrator whose output is as follows:

a. Rising linear ramp signal when - 4V is applied to it, (corresponding to binary 1).

b. Falling linear ramp signal when + 4V is applied to it (corresponding to binary 0).

The integrator output is then connected to the -ve terminal of voltage comparator, thus completing the modulator circuit.

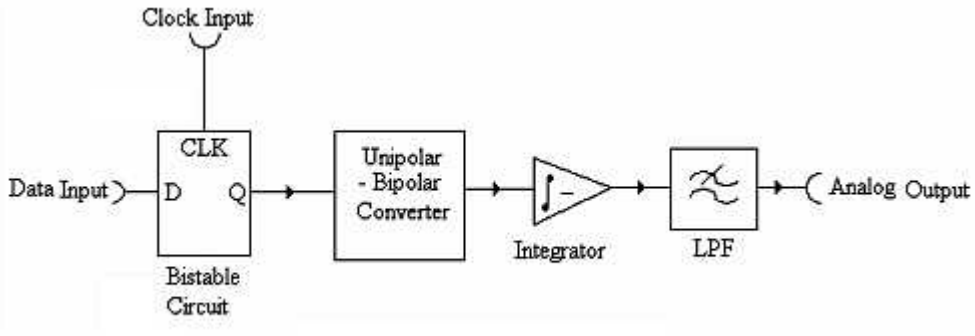
Let us understand the working of modulator circuit with the analog input waveform applied as below:



Technique of Delta Modulation

Fig. 7.2

The delta demodulator consists of a D-Flip-Flop a unipolar to bipolar converter followed by an integrator and a low pass filter. Figure 7.3 shows the block diagram of delta demodulator.



Delta De Modulator

Fig. 7.3

The delta demodulator receives the data from D-Flip-Flop of delta modulator. It latches this data at every rising edge of *receiver clock, which is delayed by half clock period with respect to transmitter clock.* This has been done so that the data from transmitter may settle down before being latched into the receiver Flip-Flop.

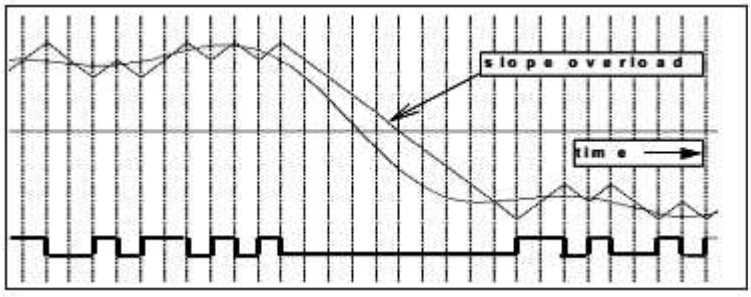
The unipolar to bipolar converter changes the output from D-Flip-Flop to either - 4V or + 4V for logic '1' and '0' respectively.

In case of modulator when the output from unipolar to bipolar converter is applied to integrator, its output tries to follow the analog signal in ramp fashion and hence is a good approximation of the signal itself. The integrator's output contains sharp edges, which are 'smoothened out' by the low - pass filter, whose cut-off frequency is just above the audio band.

The unwanted products of the modulation process, observed at the receiver, are of two kinds. These are due to *'slope overload'*, and *'granularity'*.

Slope overload:

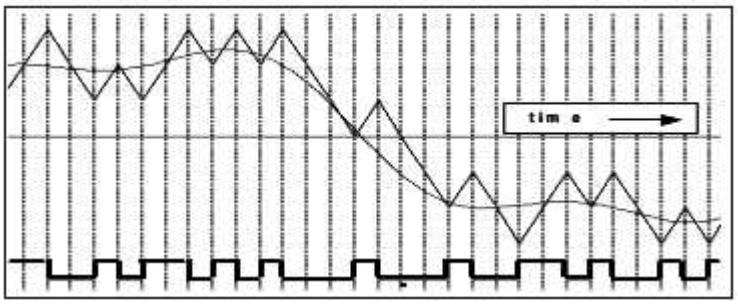
This occurs when the saw-tooth approximation cannot keep up with the rate-of-change of the input signal in the regions of greatest slope. The step size is reasonable for those sections of the sampled waveform of small slope, but the approximation is poor elsewhere. This is 'slope overload', due to too small a step. Slope overload is illustrated in Figure 7.4.



Slope overload

Fig. 7.4

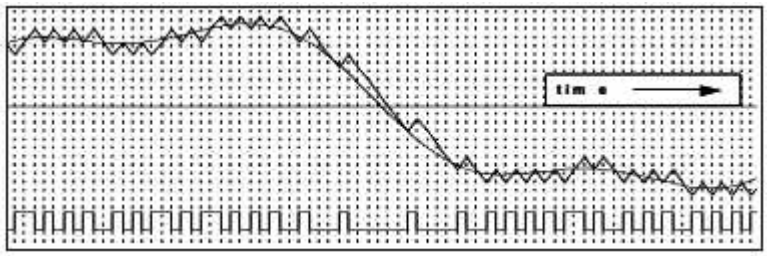
To reduce the possibility of slope overload the step size can be increased (for the same sampling rate). This is illustrated in Figure 7.5. The sawtooth is better able to match the message in the regions of steep slope.



Increased step size to reduce slope overload

Fig. 7.5

An alternative method of slope overload reduction is to increase the sampling rate. This is illustrated in Figure 7.6, where the rate has been increased by a factor of 2.4 times, but the step is the same size as in Figure 7.4.



Increased sampling rate to reduce slope overload

Fig. 7.6

Granular noise:

Refer back to Figure 7.4. The sawtooth follows the message being sampled quite well in the regions of small slope. To reduce the slope overload the step size is increased, and now (Figure 7.5) the match over the regions of small slope has been degraded. The degradation shows up, at the demodulator, as increased quantizing noise, or 'granularity'.

Apparatus Required:

- Delta Mod/DemodKit (ST2155).
- A CRO / DSO

Block/Connection Diagram:

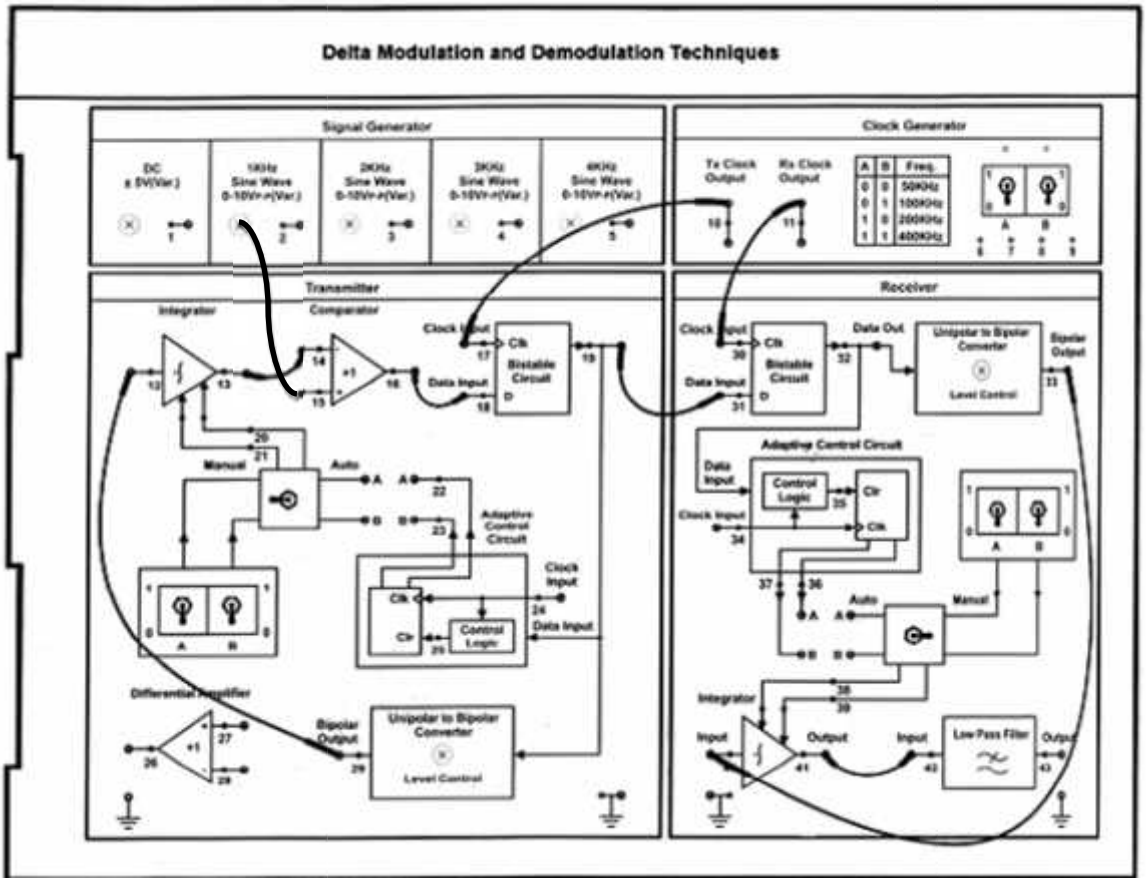


Fig. 7.7

Procedure:

Initial setup of ST2155:

Clock frequency selector switches	:	A = 0 and B = 0 position.
Integrator (1) blocks switches position:		
Gain control switch position	:	Left-hand side
Switches position	:	A=0 and B=0 position
Integrator (2) blocks switches position:		
Gain control switch position	:	Right-hand side
Switches position	:	A = 0 and B = 0 position.

1. Connect the mains supply cord to the Techbook.
2. Make connection on the board as shown in the figure 7.7.
3. Switch 'ON' the techbook power supply and oscilloscope.

4. **In order to ensure for correct operation of the system, we first take the input to 0V**. So connect the '+' input of the delta modulator's voltage comparator to 0V and monitor on an oscilloscope the output of integrator 1 (TP13) and the output of the transmitter's unipolar to bipolar converter (TP 29)
   If the transmitter's unipolar to bipolar converter output has equal positive and negative output levels, integrator's output will be a triangular wave centered around '0' Volts, as shown in figure 7.8(Case A). However, if the unipolar to bipolar converter's negative level is greater than the positive level, the integrator's output will appear as shown in figure 7.8 (Case B). Should the unipolar to bipolar converter's positive output level be the greater of the two levels, the integrator's output willresemble that shown in figure 7.8(Case C).
5. The relative amplitudes of the unipolar to bipolar converter's positive andnegative output levels can be varied by adjusting the level adjust preset in theunipolar to bipolar converter circuit 1 block. When it is turned anticlockwise,the negative level increases relative to the positive level, whenturnedclockwise, the positive level increases relative to the negative level.Prove that you can obtain all the three waveforms shown in figure 7.8 byturning the potentiometer from one extreme to another. Try explaining thereason behind it.

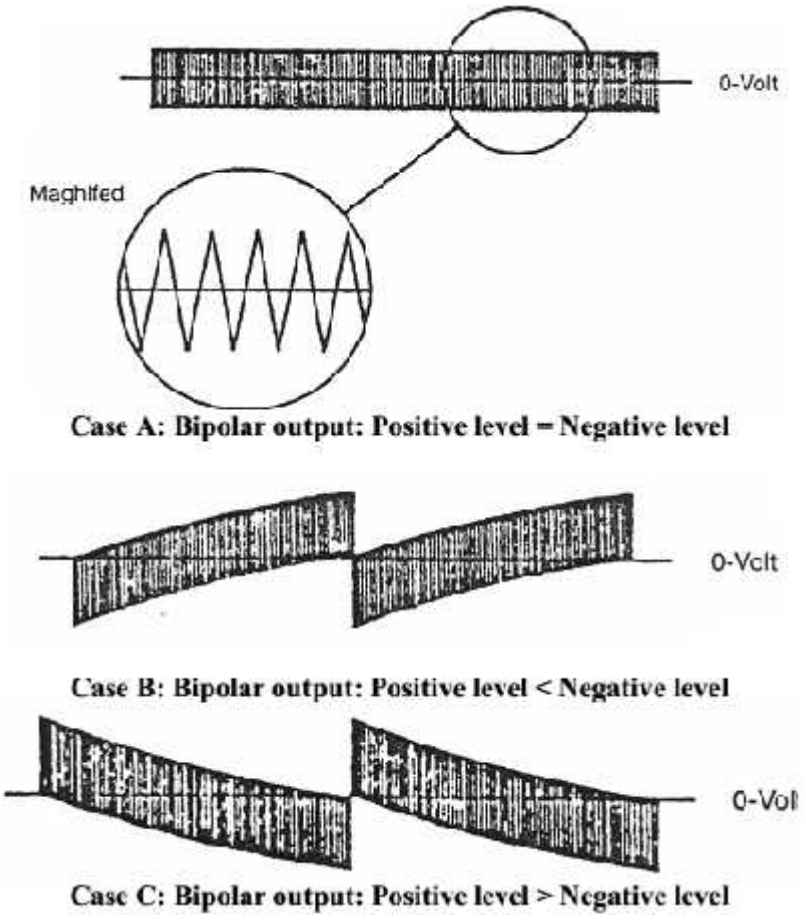


Fig. 7.8

6. Adjust the transmitter's level changer preset until the output of integrator 1 (TP 13) is a triangular wave centered around 0 Volts, as shown in figure 7.8(Case A). The peak-to-peak

amplitude of the triangle wave at the integrator's output should be 1.8V (approx), this amplitude is known as the *integrator step size.* The output from the transmitter's bistable circuit (TP 19) will now be a stream of alternate '1' and '0', 's' this is also the output of the delta modulator itself. The delta modulator is now said to be 'balanced' for correct operation.

7. Examine the signal at the output of integrator 2 (TP 41) at the receiver. This should be a triangular wave, with step size equal to that of integrator 1, and ideally centre around 0 Volts. If there is any DC bias at the output of integrator 2, remove it by adjusting the receiver's level adjust preset (in the unipolar to bipolar converter circuit 2 block). This preset adjusts the relative amplitudes, of the positive and negative output levels from the receiver's unipolar to bipolar converter circuit. Only when these levels are balanced will there be no offset at the output of integrator2.

8. Outputs at TP 13 and TP 41 respectively

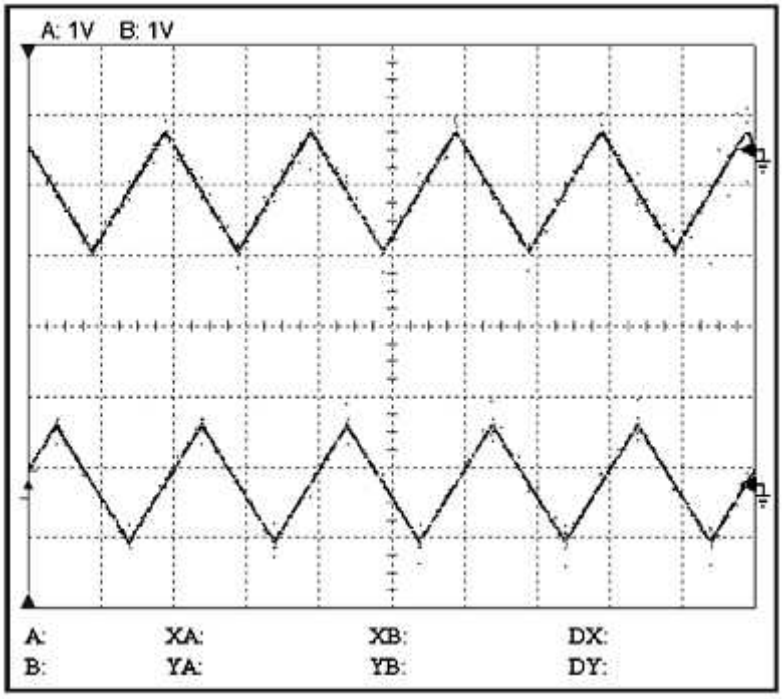


Fig. 7.9

The receiver's low pass filter (whose cut off frequency is 4.2 KHz.) then filters out the higher - frequency triangular wave, to leave a DC level at the output of filter (TP 43). If the receiver's level adjust preset has been adjusted correctly, this DC level will be '0' volt. The delta demodulator also is now balanced for correct operation.

9. **Disconnect the voltage comparators '+' input from 0V, and reconnect it to the ~1 KHz output from the function generator block**; the modulator's analog input signal is now a 1 KHz sine wave.
   Monitor this analog signal at the voltage comparator's '+' input (TP 15) together with the output of, integrator 1 (TP 13).Trigger the scope on the same analog signal which is applied to the voltage comparator's '+' input (TP 15). Note how the output of the transmitter integrator follows the analog input
   Note :- It may be necessary to readjust slightly the transmitter's level adjust preset (in the unipolar to bipolar converter circuit 1 block) in order to obtain a stable, repeatable trace of the integrator's output signal.
10. Display the data of the transmitter's bistable (at TP 19), together with the analog input at TP 15 (again trigger on this signal), and note that the 1 KHz sine wave has effectively been encoded into a stream of data bits at the bistable's output, ready for transmission to the receiver.
11. For a full understanding of how the delta modulator works, examine the output of the voltage comparator (TP 16), the bistable's clock input (TP 19), and the unipolar to bipolar output (TP 29)
12. Display the output of integrator 1 (TP 13) and that of integrator 2 (TP 41) on the scope. Note that the two signals are very similar in appearance, showing that the demodulator is working as expected.
    Outputs at TP 13 and TP 41 respectively

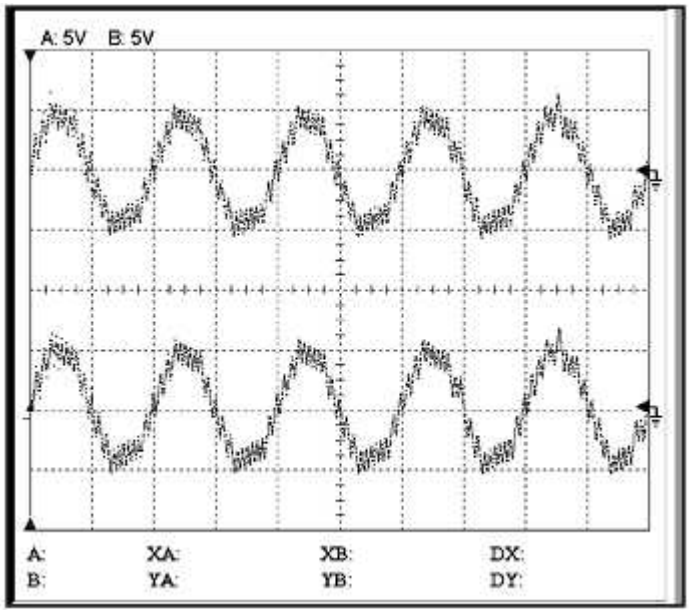


Fig. 7.10

13. Display the output of integrator 2 (TP 41) together with the output of the receiver's low pass filter block (TP43). Note that although the integrator's output has been smoothed out somewhat by the low pass filter, some unwanted 'ripple' still remains at filter's output This 'ripple' is due to the 'quantization noise' at the integrator's output, which is caused by the

relatively large integrator step size. This step size can be reduced by increasing the rate at which the system is clocked (i.e. the sampling frequency).This reduces the sampling period, and hence the time available between samples for the integrators to ramp up and down.

14. The current system clock frequency is 50 KHz. This is set by the A, B switches in the clock frequency selector block, which are currently in the A= 0, B= 0 positions. While monitoring the same signals, increase the system clock frequency to 100 KHz, by putting the switches in the A = 0, B = 1 positions.

Note :- If the integrator's output (TP41) no longer gives a stable trace after changing the clock frequency, make a slight adjustment to the transmitter's level adjust preset (in the unipolar to bipolar converter circuit 1 block), until the trace is once again stable.

Notice that, at the integrator's (TP41), the frequency of the triangular error signal doubles, and the peak-to-peak amplitude of that error signal (i.e. the step size) is halved. Examine the ripple at the low-pass filter's output (TP43). Note that this is now less than it was before.

15. By changing the system clock frequency to first 200 KHz (clock frequency selector switches in A=l, B=0 positions), and then to 400 KHz (switches in A=l, B=1 positions), note the improvement in the low - pass filter's output signal (TP43).

Once again, it may be necessary to adjust slightly the transmitter's level adjust preset, in order to obtain a stable oscilloscope trace.

16. Using a system clock frequency of 400 KHz compare the low pass filter's output (TP43) with the original analog input (TP15). There should now be no noticeable difference between them, other than a slight delay.

Output waveforms at TP15 and TP43 respectively

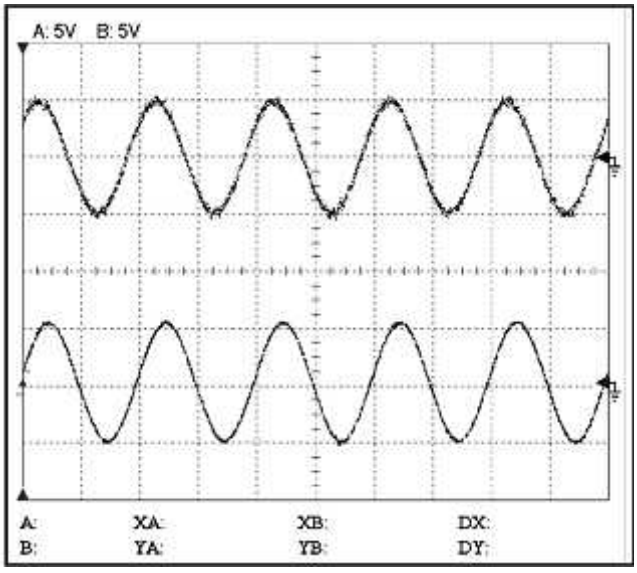


Fig. 7.11

17. While continuing to monitor the transmitter's analog input (TP15) and the receiver's low-pass filter output (TP43), **disconnect the comparator's + input from the 1 KHz sine wave output, and reconnect it to 2 KHz, 3 KHz and 4 KHz outputs in turn and using system clock frequency of 50 KHz** . Note that, as the frequency of the analog signal increases, the low pass filter's output becomes more distorted and reduced in amplitude.

18. In order to understand what has caused this distortion, **leave the comparator's + input connected to the 1 KHz sine wave output of the function generator**, and examine the output of integrator 2 (TP41). Note that the integrator's output no longer approximates the analog input signal, but is triangular. Compare this with the output of integrator 1 (TP13), and note that the two signals are exactly the same; the problem obviously starts in the delta modulator circuit

Output waveforms at TP13 and TP41 respectively

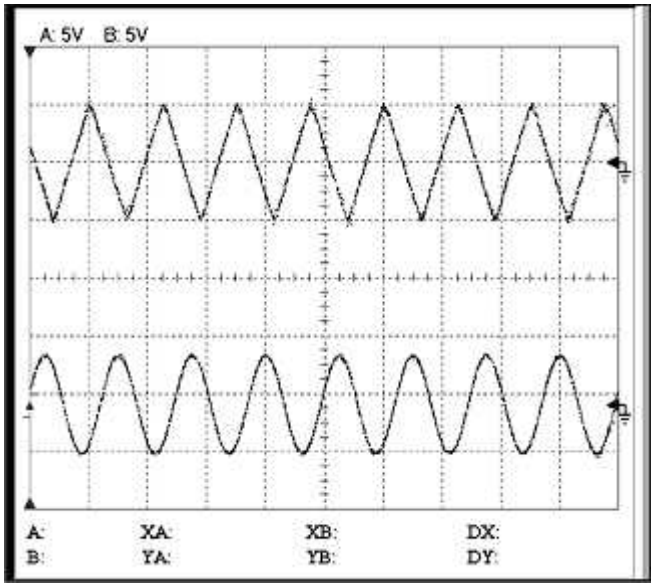


Fig. 7.12

19. Compare the 4 KHz analog input signal (TP15) with the output of integrator 1 (TP13) it should now become clear what has happened. The analog signal is now changing so quickly that the integrator's output cannot ramp fast enough to 'catch up' with it, and the result is known as '*slopeoverloading.*'

20. Although the system clock frequency i.e. the sampling frequency determines how often the integrator's output direction can change (up or down), it does not affect how quickly the integrator's output can ramp up and down. Consequently, changing the system clock frequency will not help the slope overload problem. Prove this by changing the clock frequency selector switches, and noting that the problem is still present.

Return the switches to the A= 1, B=1 (400 KHz clock frequency) position before continuing.

21. If slope overloading is to be avoided in a practical delta modulation system, the transmitter integrator must be able to ramp up or down at a rate which is at least as great as the

maximum rate of change at the transmitter's analog input. If the incoming analog signal is a sine wave, its maximum rate of change occurs at the zero crossing point, and is proportional to both the frequency and the amplitude of the sine wave.

Hence, the likelihood of slope overloading can be reduced by either reducingthe maximum input frequency, or by reducing the maximum input amplitude tothe delta modulator. We have already seen how slope overloading can beavoided by reducing the frequency of the analog input signal since there was noproblem with the ~1 KHz analog input. Now check that the problem can also beavoided if the amplitude of the input signal is reduced. Do this by slowlyturning the ~4 KHz preset anticlockwise.

Note that there comes a time when the integrator's output can once again followthe analog input signal.

22. Another possible way of overcoming slope overloading is to increase the gain of the integrators so that they can ramp up and down faster, and so can follow even those analog input waveforms those change very quickly. To illustrate this, first return the ~4 KHz preset to its clockwise (maximum amplitude) position, so that slope overloading can once again be seen on the scope.

In each of the two integrator blocks, there are two switches labeled A and B. The 2bit binary code produced by these switches selects one of four integrator gains, the lowest gain selected when the switches are in the A=0, B=0 positions. For each increasing step, in the switch code, A=0, B=0 to A=1, B=1, the integrator gain is doubled.

Output waveforms at TP15 and TP43 respectively

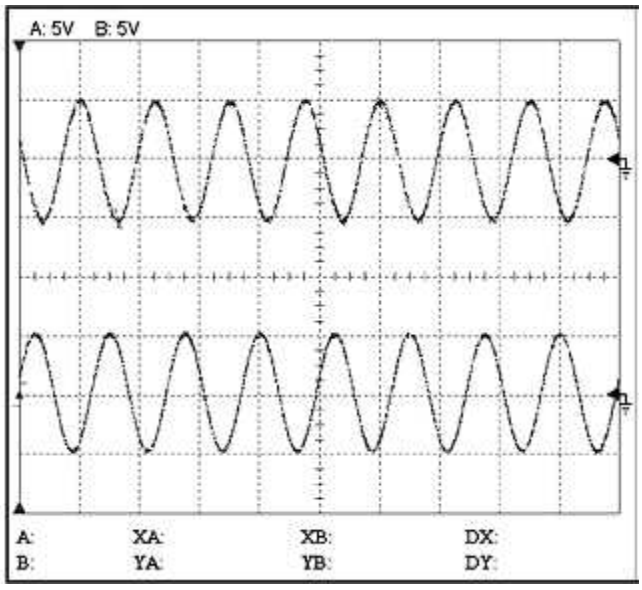


Fig. 7.13

Change the codes produced by the switches (in both integrator 1 and integrator 2 blocks) from A= 0, B=0 to A = 1, B=1, to double the gain of the two integrators; note that slope overloading still occurs. Then change both sets of switches to the A = 1, B = 0 position, and finally to the A=1, B= 1, position, to show that slope overloading can be eliminated if the integrator gain is large enough. Once again, it may be necessary to make a slight adjustment to the transmitter's level adjust preset, in order to obtain a stable trace on oscilloscope.

Note that, although it is the gain of integrator 1 alone which determines whether or not slope overloading will occur, integrator 2 must have the same gain if the amplitude of the demodulator's analog output is to be equal in amplitude to the modulator's analog input.
Output waveforms at TP15 and TP43 respectively

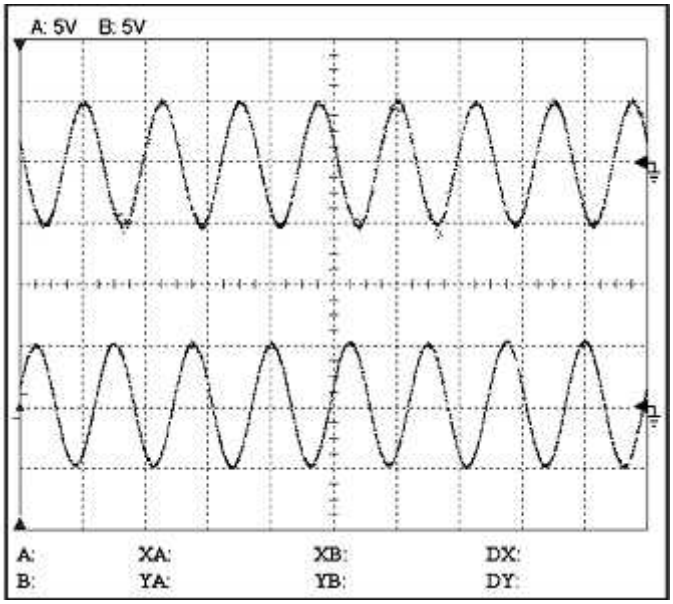


Fig. 7.14

Observations:

We have observed slope over loading can be overcome by changing anyone of the three following options:

- **a.** Reducing the maximum input frequency to the delta modulator.
- **b.** Reducing the maximum input amplitude, or
- **c.** Increasing the integrator gain.

In a practical delta modulation communication system, the signal at the modulator's analog input would normally be in the audio band, so that the maximum input frequency could not be reduced below about 3.4 KHz without losing information. This rules out solution (a) above.
The problems with reducing the amplitude of input signal i.e. solution (b) is that smaller input signals then are lost in the quantization noise. They become smaller in amplitude than the integrator's step size.

Observation Table:

Clock Frequency Applied for TX &Rx:

Sl. No.	Applied Input		Output
	I/P Frequency	I/P Voltage	O/P voltage
1	0 KHz		
2	1 KHz		
3	2 KHz		
4	3 KHz		
5	4 KHz		

Discussion&Conclusions:

Write briefly your comments about the above experiment.

Some Sample questions:

1. What is delta modulation?
2. What is the slope overloading?
3. How over slope overloading can be reduced?
4. What is the function of unipolar to bipolar circuit?
5. What is the function of integrator?
6. Implement **DM** modulation scheme using a suitable input sinusoidal signal. Trace integrator output, modulator output and demodulator output and demodulated waveforms. Discuss the results.

EXPERIMENT # 7A

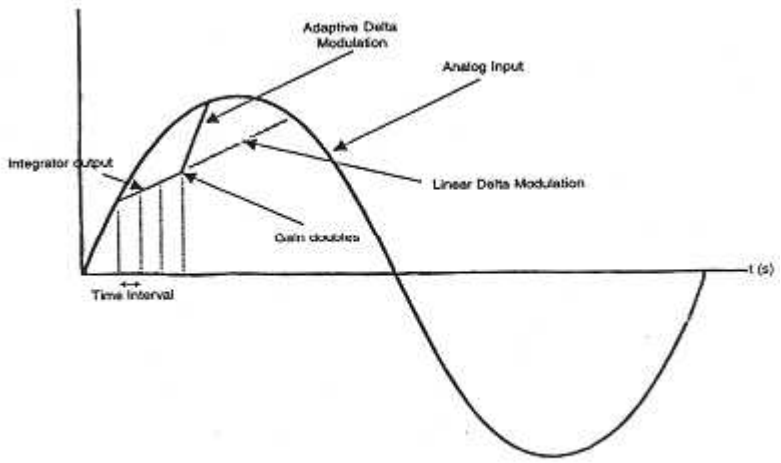
Title: STUDY OF ADAPTIVE DELTA MODULATION AND DEMODULATION TECHNIQUES

Objective:

- Study of Adaptive Delta modulator and demodulator.

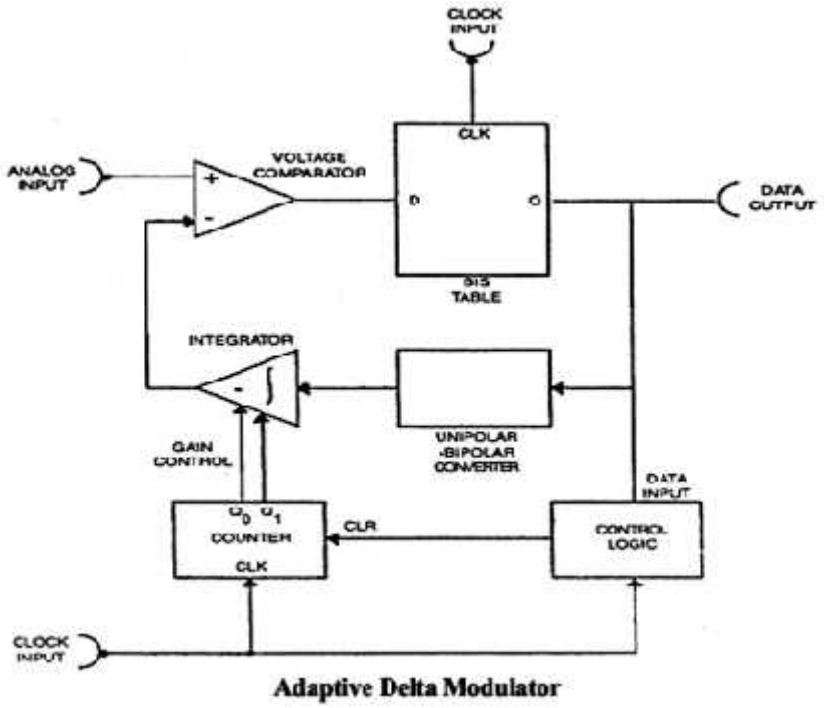
Theory:

Delta modulation system is unable to chase the rapidly changing information of the analog signal, which gives rise to distortion & hence poor quality reception. This is known as slope overloading phenomenon. The problem can be overcome by increasing the integrator gain (i.e. step-size). But using high step-size integrator would lead to a high quantization noise.



Principal of Adaptive Delta Modulation

Fig. 7.1a



Adaptive Delta Modulator

Fig. 7.2a

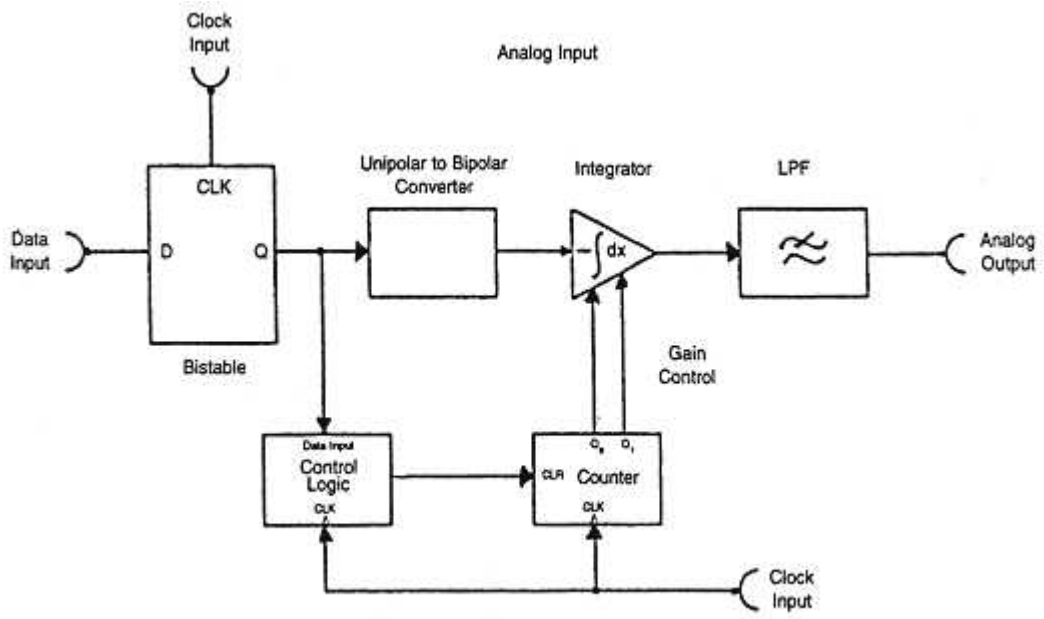
The adaptive delta modulator works as Follows:

The control circuit compares the preset data bit from D flip-flop with the previous two data bits. Its output to the counter is high when the three bits are identical, the control circuits output goes low, thus letting the counter advance with every clock cycle. This advancement continues till the output from the control circuit does not go 'high'. Each time the counter is incremented from '00' integrator gain is doubled till the counter reached '11' where it remains in that state until it is reset by the counter. Similarly, the adaptive delta demodulator is a like delta demodulator except for two blocks namely, the control circuit & the counter. They function in the same way as in modulator part, except for the fact that they are clocked by the receiver clock. Consider the adaptive delta modulator in operation. In normal case, when slope overloading is not occurring, the integrator output always hunt above & below the analog input even after it has caught up with it. The output from the D-Flip-Flop is a constantly changing from ' l' to '0' at each TX clock edge. Even when the analog input is changing at a slightly higher rate, the integrator ramp output is able to catch it in two clock cycles. Thus, the output of the D-Flip-Flop is never a three or more consecutive '0' or '1's.

The changing input to the control circuit ensures that its output to the counter is high & hence the counter is reset at every clock cycle. Thus the control word from counter is always '00' forcing the integrator gain at its lowest value, thereby reducing quantization noise. Here the adaptive delta modulator is behaving just as a delta modulator.

Suppose, now a fast changing analog signal appears at the input of the modulator such that the slope overloading occur. The integrator output no longer follows the analog signal but it spends its

time trying to catch up the analog signal (either it ramps down or up continuously). As a result of continuous ramping in one direction, the D-Flip- Flops output is either '0' or '1' for three or more consecutive time. As soon as the third continuous 1/0 is sensed by the control circuit its output goes low. The counter now advances to 01 doubling the integrator gain. This increases the ramping rate of the integrator & it is able to catch the analog signal faster. In the next clock cycle if the same situation continues the counter advances to '10' thus forcing the integrator gain to quadruple its standard value. This situation continues till the counter advances to '11' where it remains locked until the control logic does not detect a change in the bit level at its input As soon as the control circuit detects a change in the bit level, its output goes high, thus resting the counter & thus normalizing the integrator gain.



Delta Adaptive Demodulator

Fig. 7.3a

The Demodulator work as follows:

The adaptive delta demodulator control circuit receives the same bit stream as the transmitted one except for the fact that it is received after a half clock cycle delay. The functioning of the receiver's control circuit & counter is same as that of the transmitter's block. Therefore, the demodulator output which itself is a good approximation of the analog input signal accepts for the inhere spikes. The output from integrator is passed to a low pass filter to 'smooth out 'the waveform. Thus, adaptive delta modulation system is thus able to reduce slope-over load error at an expense of small increase in quantization error. It turns out that in matter of speech transmission the reduced slope error provides a net advantage in spite of slight increase in quantization error & that the adaptive delta.

Modulator can operate at the bit rate of 32 KB/S with performance comparable to that obtained using PCM at 64 KB/S.

Apparatus Required:

- Delta Mod/DemodKit (ST2155).
- A CRO / DSO

Block/Connection Diagram:

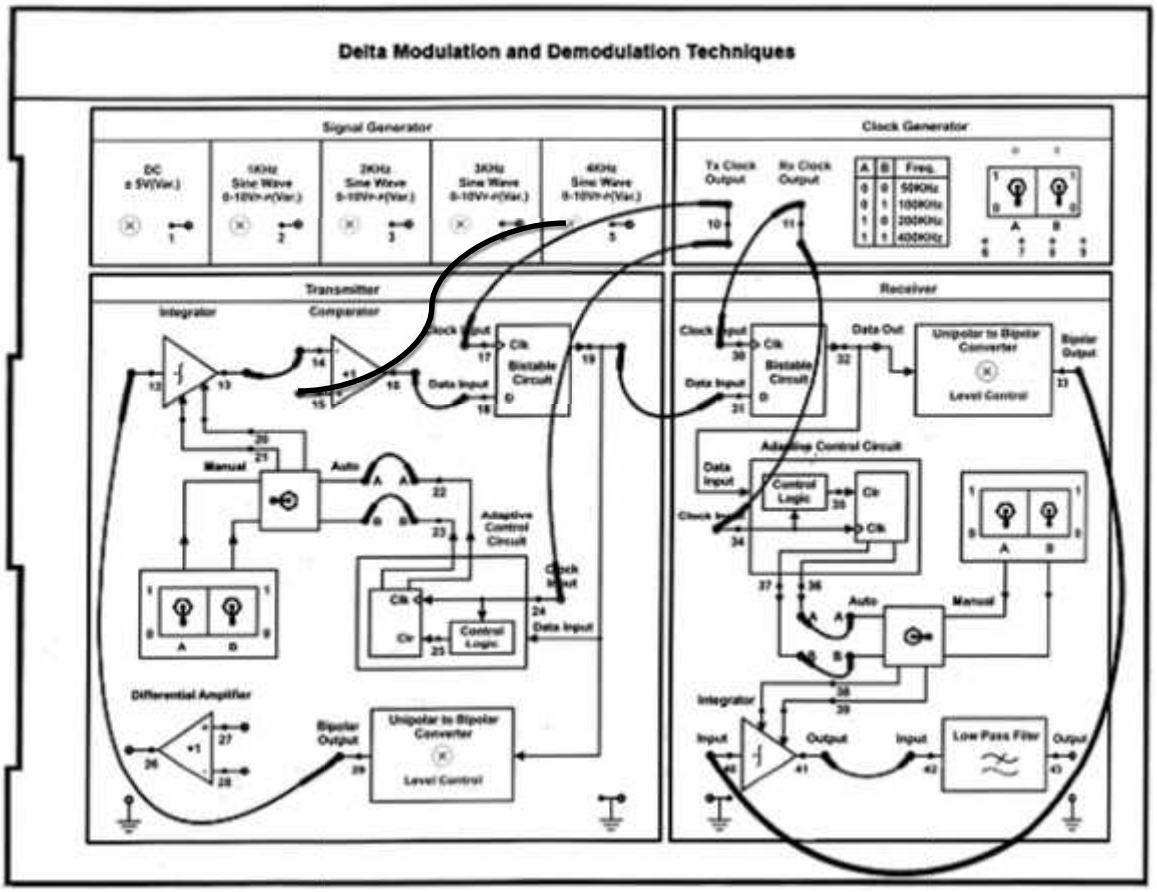


Fig. 7.4a

Procedure:

Initial setup of ST2155:

Clock frequency selector switches	:	A = 0 and B = 0 position.
Integrator (1) blocks switches position:		
Gain control switch position	:	Left-hand side
Switches position	:	A=0 and B=0 position
Integrator (2) blocks switches position:		
Gain control switch position	:	Right-hand side
Switches position	:	A = 0 and B = 0 position.

Function Generator's potentiometers position:
1 KHz to 4 KHz Pots position : fully clockwise position

1. Connect the mains supply cord to the Techbook.
2. Make connection on the board as shown in the figure 7.4a.
3. Switch 'ON' the techbook power supply and oscilloscope.
4. As the gain control switch is towards A & B switches, the gain setting is still manual, **connect the voltage comparator's +ve input to 0V & check whether the modulator & demodulator are balanced for correct operation as in delta modulation experimentation**. Change the clock frequency selector switches to the A=1, B=1, positions (400 KHz Clock Frequency) before continuing.
5. **Disconnect the voltage comparators '+' input from 0V and reconnect it to the 4 KHz output from the function generator block.**
6. Monitor the 4 KHz analog input at TP14 and the output of integrator 1 at TP13. Note that slope overloading is still occurring, as indicated by the fact that the integrator's output is not an approximation of the analog input signal.
7. At the transmitter, move the slider of the gain control switch in the integrator 1 block to the right-hand position (towards the sockets labeled A, B). At the receiver, move the slider of the gain control switch in the integrator 2 block to the left-hand position (again towards the sockets labeled A, B). The gain of each integrator is now controlled by the outputs of the counter connected to it. Functionally, the transmitter and receiver are now configured as shown in the figure 7.2a&7.3a i.e. as adaptive delta modulator and demodulator respectively.
8. Once again examine the 4 KHz analog input at TP14 and the output of integrator 1 at TP13, noting that the" slope overloading problem has been eliminated, and that the integrator's output once again follows the analog input signal. Again, it may be necessary to adjust slightly the transmitter's level adjust preset, in order to obtain a stable trace of the integrator's output signal.
9. Compare the output of integrator 1 (TP13) with that of integrator 2 (TP41); noting that, both are identical in appearance as expected.
   Output waveforms at TP13 and TP43 respectively

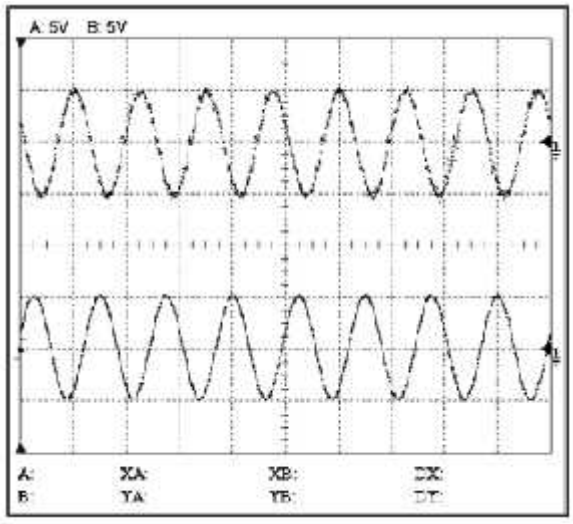
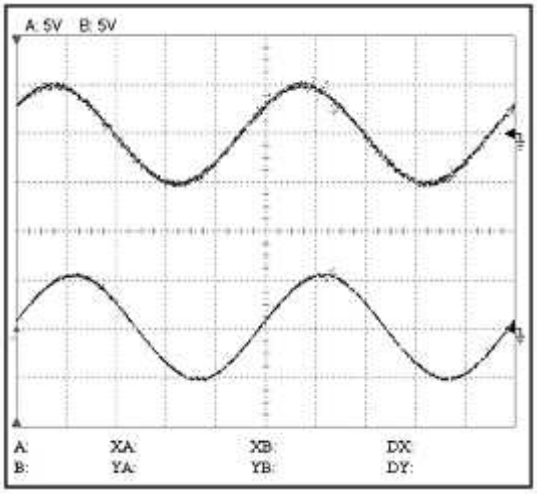


Fig. 7.5a

10. Examine the output of the low pass filter (TP42) and the output of integrator 2(TP41). The filter has removed the high-frequency components from the integrator's output signal, to leave good, clean 4 KHz sine wave.

11. Compare the original 4 KHz analog input signal (at TP15) with the output signal from the receiver's low pass filter at TP43).
Note that the demodulator's output signal is identical to the modulator's input signal, but is delayed somewhat.

12. Disconnect the voltage comparator's '+' input from the 4 KHz function generator output, and reconnected it in turn to the 3 KHz, 2 KHz and 1 KHz outputs, noting in each case that the demodulator's output signal is identical to the modulator's input signal, but delayed in time.
Output waveforms at TP13 and TP43 respectively.



1. Fig. 7.6a

13. The adaptive delta modulator/demodulator system has therefore eliminated slope-overloading problems. To examine in details how it does this, reconnect the voltage comparator's '+' input to the function generator's 4 KHz output, then reduce the system clock (i.e. sampling) frequency to 50 KHz, by putting the clock frequency selector switches in the A=0, B=0 positions. Although a 50 KHz sampling frequency is too low to ensure that an undistorted output is obtained from the demodulator's low pass filter, it does increase the step size to a level, which makes it easier to understand how the system is operating.

14. Monitor the 4 KHz analog input signal at TP14 and at the output of integrator 1 (TP13). It should now become a little clearer as to how the adaptive delta modulator is operating. It will be noted that the slope of the integrator's output signal is no longer constant, but increases in a series of discrete steps, in order to 'catch up' with the fast-changing analog input signal.
If the integrator output does not 'catch up' with the analog input within two clock periods of its direction changing, the slope of the integrator's output signal. (i.e. the integrator gain) is doubled. If it has still not caught up with the analog input signal by the end of the third clock period, the integrator gain will double once again. If the integrator output still lags behind at the end of the fourth clock period, the integrator's gain is doubled once again,

toits maximum value. It then remains at this value until the integrator output 'catches up' with the analog input signal. Once the integrators output 'overtakes' the analog input signal, its direction changes, and its rate of change reverts to the minimum value.

15. Examine also the test points in the adaptive control circuit 1 block (TP22-25), to have an understanding of how the adaptive delta modulator is operating.

16. While monitoring the outputs of the modulator's binary counter (TP22 and 23), slowly turn the 4 KHz preset anticlockwise, in order to reduce the amplitude of the 4 KHz analog input signal. Notice that once the analog input signal becomes small enough, both the counter's outputs becomes permanently low, causing the integrator to have minimum gain. This happens because the input signal is now so small that the integrator can always follow it, even with minimum gain. The result is that small-amplitude input signals can be transmitted with minimum integrator gain, thereby keeping quantization noise to a minimum at the demodulator's output.

Observation Table:

Clock frequency applied for Tx and Rx:

Sl. No.	Applied Input		Output
	I/P Frequency	I/P Voltage	O/P voltage
1	0 KHz		
2	1 KHz		
3	2 KHz		
4	3 KHz		
5	4 KHz		

Discussion&Conclusions:

Write briefly your comments about the above experiment.

Precautionary Measure to be taken:

1. Ensure that equipment or training kit switch is kept off. While connecting it to main power supply.
2. For connecting any signal from one equipment to another equipment or from one section to other section of the same kit, ensure that signal is grounded properly and subsequently connect the signal-to-signal line.
3. Handle gently all the necessary button or knob in the equipment avoiding all other buttons or knobs which are not required to be adjusted for the equipment.
4. For unusual spark or burning smell, immediately switch off the main supply to the kit.
5. Ensure that, a signal is connected to an appropriate junction destined for it.
6. Always cover the equipment for dust protection after the experiment.

Some Sample questions:

1. What is adaptive delta modulation?
2. What is the drawback of delta modulation?
3. What is the effect of frequency on adaptive delta modulation?
4. What is advantage of adaptive delta modulation?
5. Why integrator is required for adaptive modulation?
6. Implement ADM modulation scheme using a suitable input sinusoidal signal. Trace integrator output, modulator output and demodulator output and demodulated waveforms. Discuss the results.

EXPERIMENT # 8

Title: STUDY OF PN SEQUENCE

Objective:

- To generate PN Sequence
- To verify the Property of Balance
- To verify the property of time shifted PN Sequences
- To verify Shift and Add Property
- To find the Auto Correlation Function
- To find Cross Correlation Function
- To check orthogonality of PN Sequence

Theory:

A Pseudo-random Noise (PN) sequence is a sequence of binary numbers, e.g. ±1, which appears to be random; but is in fact perfectly deterministic. The sequence appears to be random in the sense that the binary values and groups or runs of the same binary value occur in the sequence in the same proportion they would if the sequence were being generated based on a fair "coin tossing" experiment. In the experiment, each head could result in one binary value and a tail the other value. The PN sequence appears to have been generated from such an experiment. A software or hardware device designed to produce a PN sequence is called a PN generator.

Pseudo random noise sequences or PN sequences are known sequences that exhibit the properties or characteristics of random sequences. They can be used to logically isolate users on the same frequency channel. They can also be used to perform scrambling as well as spreading and dispreading functions.

The reason we need to use PN sequences is that if the code sequences were deterministic, then everybody could access the channel. If code sequences were truly random on the other hand, then nobody, including the intended receiver, would be able to access the channel. Thus using a pseudo random sequence makes the signal look like random noise to everybody except to the transmitter and the intended receiver.

PN Sequences and Generators

A PN generator is typically made of N cascaded flip-flop circuits and a speciallyselected feedback arrangement as shown below.

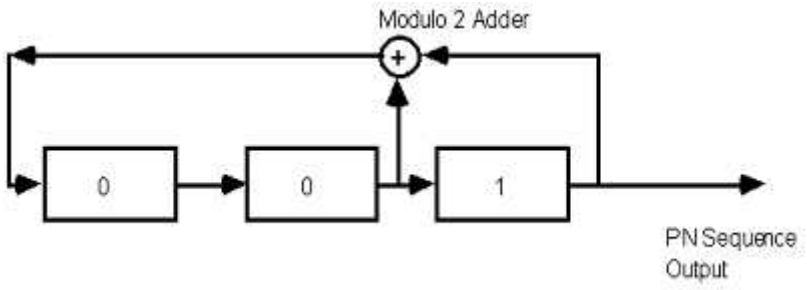


Fig.8.1

The flip-flop circuits when used in this way is called a shift register since each clock pulse applied to the flip-flops causes the contents of each flip-flop to be shifted to the right. The feedback connections provide the input to the left-most flip-flop. With N binary stages, the largest number of different patterns the shift register can have is 2N.
However, the all-binary-zero state is not allowed because it would cause all remaining states of the shift register and its outputs to be binary zero. The all-binary-ones state does not cause a similar problem of repeated binary ones provided the number of flipflops input to the module 2 adder is even. The period of the PN sequence is therefore 2N-1, but IS-95 introduces an extra binary zero to achieve a period of 2N, where N equals 15.
Starting with the register in state 001 as shown, the next 7 states are 100, 010, 101, 110, 111, 011, and then 001 again and the states continue to repeat. The output taken from the right-most flip-flop is 1001011 and then repeats. With the three stage shiftregister shown, the period is **(2^3-1)** or 7. The PN sequence in general has 2N/2 binaryones and [2N/2]-1 binary zeros. As an example, note that the PN sequence 1001011 ofperiod **(2^3-1)**contains 4 binary ones and 3 binary zeros.

PN Sequences also referred to as PN Codes sequences can be generated with an n-stage Linear Shift Register where:

1. Appropriate taps are connected to a Modulo 2 adder;
2. A seed pattern (other than an all-zeros state) is continuously shifted through the Linear Shift Register, triggered by a clock

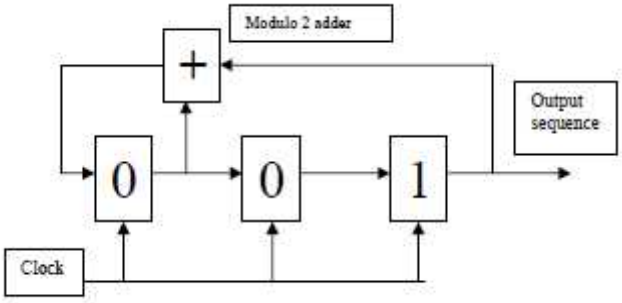


Fig.8.1

The output of the Modulo 2 adder is used to drive the input of the shift register.
Let us conduct the following experiment and draw some useful conclusions from its results:

1. Connect Tap #1 and Tap #3 to the input of the Modulo-2 adder.
2. Drive the Linear Shift register with a clock.

The resulting States of the Shift Register for various clocks are:

Clock	
0	001
1	100
2	110
3	111
4	011
5	101
6	010
7	**001**

The output sequence **1 0 0 1 1 1 0 …. (a)** Repeats itself after 7 shifts and is referred to as a PN Sequence or PN Code.

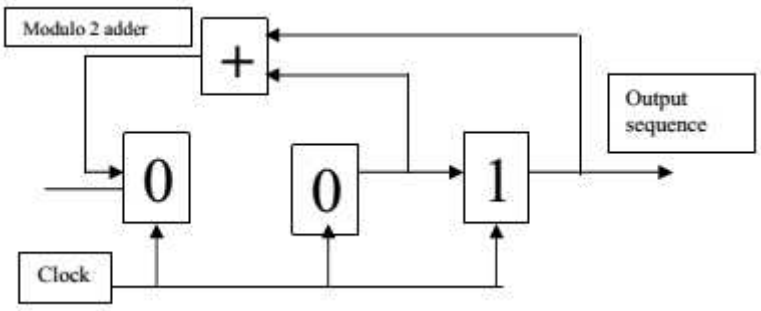


Fig.8.2

Let us conduct a second experiment similar to the first experiment with the exception of the Taps Connections:

1. Connect Tap #2 and Tap #3 to the input of the Modulo-2 adder.

The resulting States of the Shift Register for various clocks are:

Clock	
0	001
1	100
2	010
3	101
4	110
5	111
6	011
7	**001**

The output sequence Cj(t) = **1 0 0 1 0 1 1……(b)** repeats itself after 7 shifts and is referred to as a PN Sequence or PN Code

- **Length of PN Sequences:**

In general, it can be demonstrated that the Maximum Length of a PN Sequence generated by an N-stage Linear Shift Register is:

- $L=2^N-1$
- Where N is the number of stages of the Linear Shift Register.

- **PN Codes Properties:**

  - ***The Property of Balance:***

Consider the PN sequences and generated previously:

1. 1 0 0 1 1 1 0…… (a)
2. 1 0 0 1 0 1 1…… (b)

It can be demonstrated that the ratio of "ones" and "zeros" in a Maximum Length PN Sequence is as follows:

1. Number of "ones" = $2^N/2$
2. Number of "zeros" = $2^N/2$ -1
3. Where N is the number of stages of the Linear Shift Register

In our examples, and are generated by a three-stage Linear Shift Register. Therefore:

1. Number of "ones" = $2^3/2 = 4$
2. Number of "zeros" = $(2^3/2)$ -1 = 3

  - ***Time-Shifted PN Sequences***

Consider two consecutive cycles of the PN Sequence (a)
(a) = 1 0 0 1 1 1 0 **1 0 0 1 1 1 0**
Now, let us shift, (to the left side), a (t) and observe the various shifted sequences as a function of the shift or delay parameter (t). The incremental time-shift is the duration of one chip.

Clock Cycle	Time-Shifts
0	1 0 0 1 1 1 0 1 0 0 1 1 1 0
1	0 0 1 1 1 0 1 0 0 1 1 1 0 **1**
2	0 1 1 1 0 1 0 0 1 1 1 0 **1 0**
3	1 1 1 0 1 0 0 1 1 1 0 **1 0 0**
4	1 1 0 1 0 0 1 1 1 0 **1 0 0 1**
5	1 0 1 0 0 1 1 1 0 **1 0 0 1 1**
6	0 1 0 0 1 1 1 0 **1 0 0 1 1 1**
7	1 0 0 1 1 1 0 **1 0 0 1 1 1 0**

Once again, the sequence repeats itself after L shifts. (Here L=7).

  - ***Shift-and-ADD Property***

The Modulo-2 condition of a PN Sequence with time-shift t_i and a time shifted version of the same PN sequence with time-shift t_j, yields another time shifted version of the same PN sequence with time-shift t_k.
A $(t-ti) \oplus a(t-tj) = a(t-tk)$
For example, consider two Time-Shifted version of the previously generated
PNsequence (a): 1 0 0 1 1 1 0
$a(t-t_1)$= 0 0 1 1 1 0 1, $a(t-t_5)$= 1 0 1 0 0 1 1

a (t-t1)⊕a (t-t5)= 1 0 0 1 1 1 0 = a (t-t_0)
Once again, the sequence repeats itself after L shifts. (Here L=7).

- ***Correlation of PN Sequences***

The correlation of two random variables X (t) and Y (t), is a "Time = shift" comparison which expresses the degree of similarity or the degree of likeness between the two variables.
1. The Auto-Correlation function Rt, provides the degree of Similarity, the degree of likeness between a random variable X (t) and a time-shifted version of X (t).
For example, let:

a. X(t)= a (t)
b. X(t-ti) = a (t-ti)
c. Y(t)= a (t-ti)
d. Auto-Correlation = Rt = 1/L [.....

To get the Average value of the Cross-correlation, normalization by the sequence length L is required.
Consider a (t) and the time-shifted version of itself; say a (t-t_1)

a (t) =	1	0	0	1	1	1	0
a (t-t_1) =	0	0	1	1	1	0	1
	D	A	D	A	A	D	A

Whencorresponding bits from the two sequences have the same parity (or match eachother), wewill call the match an **Agreement "A".**
Likewise, when corresponding bits from the two sequences do not have the sameParity (do not match each other), we will call the mismatch a **Disagreement "D".**
By counting all the Agreements and all the Disagreements over the full length L ofthe sequence, a measure of correlation can be estimated as:

Correlation value (R) = Total Number of "A" - Total Number of "D"
In our case,
A = 3 and D = 4
Correlation = A - D = -1

If the sequence is correlated with itself, the result is referred to as **auto correlation**. If a sequence is correlated with another sequence, the result is known as **cross correlation**. It is often desirable to use normalized correlation in our computation. We define this as under:

$$\rho = \frac{\text{Number of agreements (A)} - \text{Number of disagreements (D)}}{\text{Number of agreements (A)} + \text{Number of disagreements (D)}}$$

Consider the Reference PN code (a) and it's time-shifted versions as shown below.Now let us compute the Correlation of a (t) and a ($t-t_1$), for all suitable values of t_i(here from 0 to7).

Time Shifts	Shifted Sequences							Correlation(R)	°
Reference	1	0	0	1	1	1	0		
t_0	1	0	0	1	1	1	0	+7	1
t_1	0	0	1	1	1	0	1	-1	-1/7
t_2	0	1	1	1	0	1	0	-1	-1/7
t_3	1	1	1	0	1	0	0	-1	-1/7
t_4	1	1	0	1	0	0	1	-1	-1/7
t_5	1	0	1	0	0	1	1	-1	-1/7
t_6	0	1	0	0	1	1	1	-1	-1/7
t_7	1	0	0	1	1	1	0	+7	1

In general, it can be shown that the Full-Length Auto-Correlation function of PN Codes or PN Sequences is characterized by Large positive number equal to the length of the PN Sequence ($R = 2^n-1$) when time shift t = 0 (at t_0);
So, when normalized by the Length, the Auto-Correlation Function is equal to Unity "1" at time-shift zero. Negative One (-1) for all Time-Shifts equal or greater than the duration of one chip
So, when normalized by the length L of the PN Sequence, the Auto-Correlation is very small (-1/L) for all values of time shifts equal or greater than one chip. *In summary, the Auto-Correlation function of PN Codes is a two-value function: Its maximum value occurs when the time-shift parameter t is zero chip. For all other values of ti equal to, or greater than one chip, the correlation function is -1.*

Now consider the Reference PN Code a (t) and the time-shifted versions of another code b (t) as shown below. Let us compute the Correlation of a (t) and b ($t - t_i$), for all suitable values of t (0 to 7).

Time Shifts	Shifted Sequences							Correlation(R)	°
Reference	1	0	0	1	0	1	1		
t_0	1	0	0	1	1	1	0	+3	3/7
t_1	0	0	1	1	1	0	1	-1	-1/7
t_2	0	1	1	1	0	1	0	-1	-1/7
t_3	1	1	1	0	1	0	0	-5	-5/7
t_4	1	1	0	1	0	0	1	+3	3/7
t_5	1	0	1	0	0	1	1	+3	3/7
t_6	0	1	0	0	1	1	1	-1	-1/7
t_7	1	0	0	1	1	1	0	+3	3/7

- ***Orthogonal Sequences***

Two PN Sequences a (t) and b_j (t) are said to be Orthogonal if and only if:
1. Their respective Normalized Auto-Correlation Functions are equal to unity"1" at time-shifted zero (t_0).
2. Their Cross-Correlation Function is equal to zero for all time-shift values.
Averaged over the code Length, the Cross-Correlation function of PN Sequences is not zero. As a result, PN Sequences are not perfectly orthogonal.

Apparatus Required:

- PN Sequence Generator Kit (ST2114).
- A CRO / DSO

❖ To generate PN Sequence

Block/Connection Diagram:

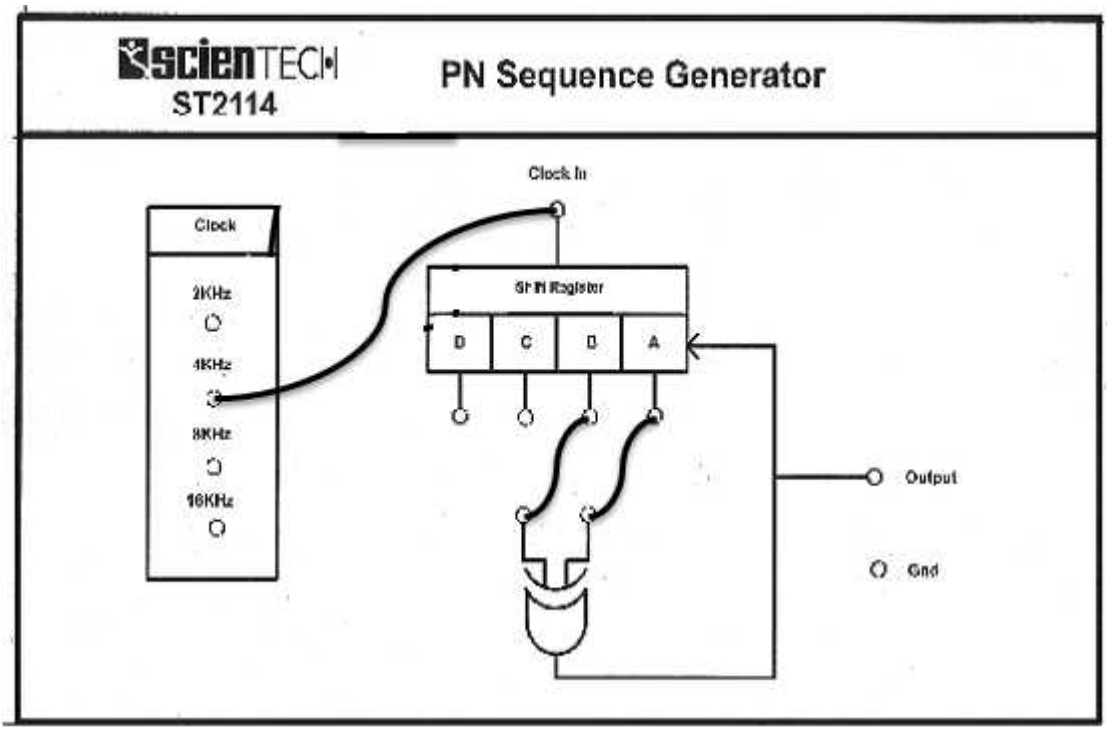


Fig. 8.3

Procedure:

1. Connect 4 KHz clock to "clock in" socket.
2. Connect 'A' socket output to any one input of EX (-) OR gate.
3. Similarly connect socket 'B' output to other input of EX (-) OR gate.
4. Switch 'On' the trainer's power supply & Oscilloscope.

5. Connect BNC connector to the CRO and to the trainer's output port.
6. Observe the output on Oscilloscope. This is the desired PN Sequence.
7. Now you can generate various sequences by selecting various combinations of shift register viz. A B C D, as input to the EX (-) OR gate.

Related Waveforms: Observed on Oscilloscope

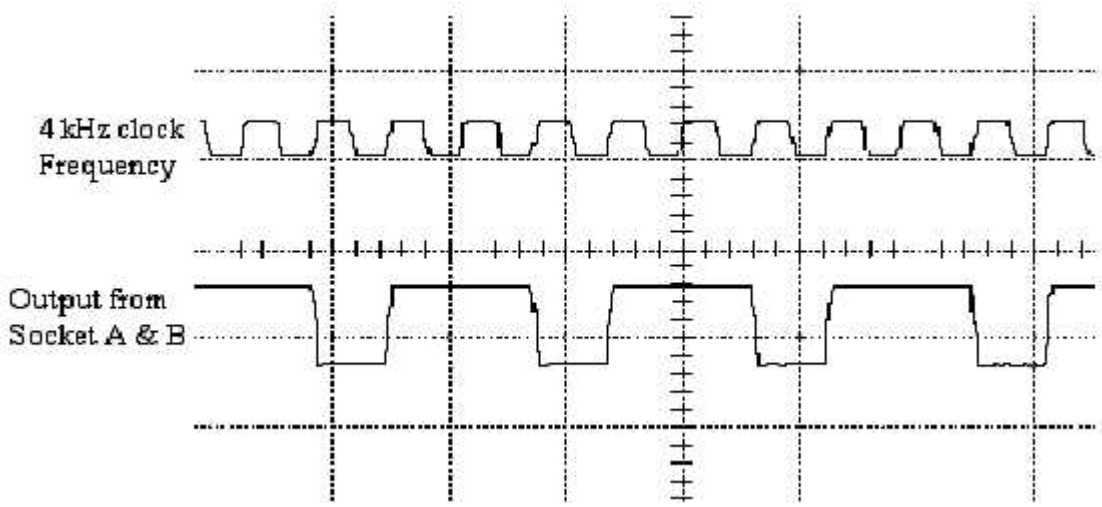


Fig. 8.4

❖ To verify the Property of Balance

Block/Connection Diagram: Fig. 8.3

Procedure:

1. Connect 4 KHz clock to "clock in" socket.
2. Connect 'A' socket output to any one input of EX (-) OR gate.
3. Similarly connect socket 'B' output to other input of EX (-) OR gate.
4. Switch 'On' the trainer's power supply & Oscilloscope.
5. Connect BNC connector to the CRO and to the trainer's output port.
6. Observe the output on Oscilloscope. This is the desired PN Sequence.
7. Now connect the input clock to second channel of Oscilloscope.
8. Count the number of zeros and ones in the data in 15 clock cycles.
9. Verify them with the formula given below:
    a. Number of "ones" = $2^N/2$
    b. Number of "zeros" = $(2^N/2)-1$
    c. Where N is the number of stages of the Linear Shift Register

❖ To verify the property of time shifted PN Sequences

Block/Connection Diagram: Fig. 8.3

Procedure:

1. Connect 4 KHz clock to "clock in" socket.
2. Connect 'A' socket output to any one input of EX (-) OR gate.
3. Similarly connect socket 'B' output to other input of EX (-) OR gate.
4. Switch 'On' the trainer's power supply & Oscilloscope.
5. Connect BNC connector to the CRO and to the trainer's output port.
6. Observe the output on Oscilloscope. This is the desired PN Sequence.
7. Now connect the input clock to second channel of Oscilloscope.
8. Consider the two consecutive cycles of PN sequence and shift them one bit at a time and write down the results in the table given below.
9. After how many clocks the sequence repeats itself?

Clock Cycle	Time-Shifts
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	

❖ To verify Shift and Add Property

Block/Connection Diagram: Fig. 8.3

Procedure:

1. Connect 4 KHz clock to "clock in" socket.
2. Connect 'A' socket output to any one input of EX (-) OR gate.
3. Similarly connect socket 'B' output to other input of EX (-) OR gate.
4. Switch 'On' the trainer's power supply & Oscilloscope.
5. Connect BNC connector to the CRO and to the trainer's output port.
6. Observe the output on Oscilloscope. This is the desired PN Sequence.
7. Observe and note the sequence. Name it x(t)
8. Now shift the sequence x (t) by one time shift and note. Name it as x $(t- t_1)$.(On Graph paper)
9. Now shift the original sequence x (t) by 4 time shift and note it. Name it x $(t-t_4)$.
10. Now EX (-) OR the two time shifted sequences viz. x (t) and x $(t-t_4)$, name the resultant sequence as x $(t-t_k)$. This is yet another time shifted sequence x (t).
11. Shift this resultant sequence and note after how many shifts does the sequencerepeats.

❖ To find the Auto Correlation Function

Block/Connection Diagram: Fig. 8.3

Procedure:

1. Connect 4 KHz clock to "clock in" socket.
2. Connect 'A' socket output to any one input of EX (-) OR gate.
3. Similarly connect socket 'B' output to other input of EX (-) OR gate.
4. Switch 'On' the trainer's power supply & Oscilloscope.
5. Connect BNC connector to the CRO and to the trainer's output port.
6. Observe the output on Oscilloscope. This is the desired PN Sequence.
7. Observe and note the sequence, call it x (t).
8. Shift the sequence by one time shift and note the resulting sequence, call it x $(t- t_1)$. (On Graph paper)
9. Find out the number of agreements 'A' and disagreements 'D' and find the correlation.
10. Normalize it with the length of sequence in our case its 15.

❖ To find Cross Correlation Function

Block/Connection Diagram: Fig. 8.3

Procedure:

1. Connect 4 KHz clock to "clock in" socket.
2. Connect 'A' socket output to any one input of EX (-) OR gate.
3. Similarly connect socket 'B' output to other input of EX (-) OR gate.
4. Switch 'On' the trainer's power supply & Oscilloscope.
5. Connect BNC connector to the CRO and to the trainer's output port.
6. Observe the output on Oscilloscope. This is the desired PN Sequence.
7. Observe and note the sequence, call it x (t).
8. Select **some other tapings of the shift register** and note the new sequence, call it y (t).
9. Shift this y (t) by one time shift, the resulting sequence will be y ($t-t_1$). (OnGraph paper)
10. Find the agreements 'A' and disagreements 'D' between x (t) and y ($t-t_1$).
11. Find out the Cross correlation by the formula given.

$$\rho = \frac{\text{Number of agreements (A)} - \text{Number of disagreements (D)}}{\text{Number of agreements (A)} + \text{Number of disagreements (D)}}$$

❖ To check orthogonality of PN Sequence

Procedure:

1. Perform experiments of **Auto Correlation and Cross Correlation**.
2. Check if the two sequence's {x (t) and y (t)}, normalized Auto-Correlation Function are equal to unity "1" at time-shifted zero (t_0).
3. Also check whether their respective Cross-Correlation Function is equal to zero for all time-shift values.
4. If the above two conditions are satisfied then the two sequences x (t) and y (t) are orthogonal.

Discussion&Conclusions:

Write briefly your comments about the above experiment.

Some Sample questions:

1. How the Length of PN Sequences is generated?
2. List PN codes properties?
3. Design and implement a circuit using universal shift register to generate PN Sequence with 4 KHz clock and verify the PN codes properties from the output.

EXPERIMENT # 9

Title: SIMULATION STUDY OF PROBABILITY OF SYMBOL ERROR FOR BPSK MODULATION

Objective:Bit Error Rate (BER) for BPSK modulation

Theory:

In digital transmission, the number of bit errors is the number of received bits of a data stream over a communication channel that have been altered due to noise, interference, distortion or bit synchronization errors.

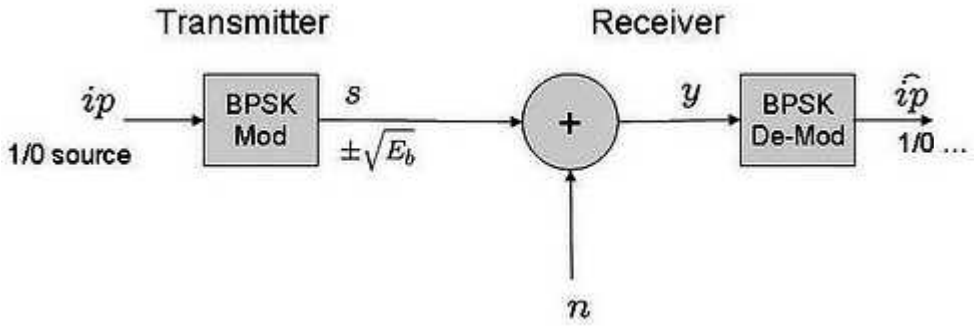
The bit error rate (BER) is the number of bit errors per unit time. The bit error ratio (also BER) is the number of bit errors divided by the total number of transferred bits during a studied time interval. Bit error ratio is a unitless performance measure, often expressed as a percentage.

The bit error probability $^{\circ}_{e}$ is the expectation value of the bit error ratio. The bit error ratio can be considered as an approximate estimate of the bit error probability. This estimate is accurate for a long time interval and a high number of bit errors.

*As an example, assume this transmitted bit sequence: [0 1 1 0 0 0 1 0 1 1] and the followingreceived bit sequence: [0 **0** 1 0 **1** 0 1 0 **0** 1], the number of bit errors (the underlined bits) is, in this case, 3. The BER is 3 incorrect bits divided by 10 transferred bits, resulting in a BER of 0.3 or 30%.*

Here the theoretical equation for bit error rate (BER) with Binary Phase Shift Keying (BPSK) modulation scheme in Additive White Gaussian Noise (AWGN) channel will be derived. The BER results obtained using MATLAB simulation scripts show good agreement with the derived theoretical results.

With Binary Phase Shift Keying (BPSK), the binary digits 1 and 0 maybe represented by the analog levels $+\sqrt{E_b}$ and $-\sqrt{E_b}$ respectively. The system model is as shown in the Figure 9.1 below.



Simplified block diagram with BPSK transmitter-receiver: Fig. 9.1

Channel Model

The transmitted waveform gets corrupted by noise n, typically referred to as **Additive White Gaussian Noise** (AWGN).

As the noise, n, gets added to the received signal, the value of noise follows the Gaussian probability distribution function given by,

$$p(n) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{\frac{-(n-\mu)^2}{2\sigma^2}} \qquad (1)$$

With $\mu = 0$ and $\sigma^2 = N_0 / 2$

The bit error probability is given by, $P(b) = \text{erfc}\left(\sqrt{\frac{E_b}{N_0}}\right)$ (2)

Computing the probability of error

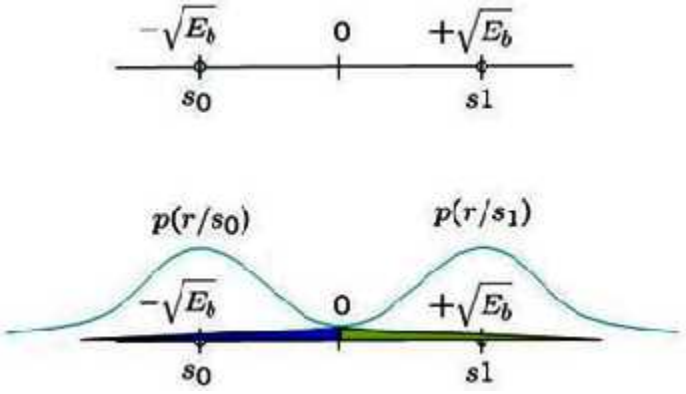
The received signal,

$y = s_1 + n$ when bit 1 is transmitted and $y = s_0 + n$ when bit 0 is transmitted

The conditional probability distribution function (PDF) of y for the two cases are

$$p(y \mid s_0) = \frac{1}{\sqrt{\pi N_0}} e^{\frac{-(y+\sqrt{E_b})^2}{N_0}}$$

$$p(y \mid s_1) = \frac{1}{\sqrt{\pi N_0}} e^{\frac{-(y-\sqrt{E_b})^2}{N_0}}$$



Conditional probability density function with BPSK modulation Fig. 9.2

Assuming that s_1 and $s_2$are equally probable i.e. $p(s_1) = p(s_0) = 1/2$, the **threshold 0** forms the optimal decision boundary.

- if the received signal is y is greater than 0, then the receiver assumes s_1 was transmitted.
- if the received signal is y is less than or equal to 0, then the receiver assumes s_0 was transmitted.
  i.e.
  $y > 0 \Rightarrow s_1$ and $y \leq 0 \Rightarrow s_0$

Probability of error given s_1 was transmitted

With this threshold, the probability of error given s_1 is transmitted is (the area in blue region): where,

$erfc(x) = \frac{2}{\sqrt{\pi}} \int_x^{\infty} e^{-x^2} dx$ is the complementary error function.

Probability of error given s_0 was transmitted

Similarly the probability of error given s_0 is transmitted is (the area in green region):

Total probability of bit error

$P_b = p(s_1)\, p(e|s_1) + p(s_0)\, p(e|s_0)$.

Given that we assumed that s_1 and s_0 are equally probable i.e. $p(s_1) = p(s_0) = 1/2$, the **bit error probability** is,

$$P(b) = \text{erfc}\left(\sqrt{\frac{E_b}{N_0}}\right)$$

Simulation model:

MATLAB source code for computing the bit error rate with BPSK modulation from theory and simulation. The code performs the following:
(a) Generation of random BPSK modulated symbols +1's and -1's
(b) Passing them through Additive White Gaussian Noise channel
(c) Demodulation of the received symbol based on the location in the constellation
(d) Counting the number of errors
(e) Repeating the same for multiple E_b/N_0 value.

MATLAB Code:-

```
clear
N = 10^6 % number of bits or symbols
rand('state',100); % initializing the rand() function
randn('state',200); % initializing the randn() function

% Transmitter
ip = rand(1,N)>0.5; % generating 0,1 with equal probability
s = 2*ip-1; % BPSK modulation 0 -> -1; 1 -> 1
n = 1/sqrt(2)*[randn(1,N) + j*randn(1,N)]; % white gaussian noise, 0dB
variance
Eb_N0_dB = [-3:10]; % multiple Eb/N0 values

for ii = 1:length(Eb_N0_dB)
   % Noise addition
   y = s + 10^(-Eb_N0_dB(ii)/20)*n; % additive white gaussian noise

% receiver - hard decision decoding
ipHat = real(y)>0;

   % counting the errors
nErr(ii) = size(find([ip- ipHat]),2);

end

simBer = nErr/N; % simulated ber
theoryBer = 0.5*erfc(sqrt(10.^(Eb_N0_dB/10))); % theoretical ber

% plot
close all
figure
semilogy(Eb_N0_dB,theoryBer,'b.-');
hold on
semilogy(Eb_N0_dB,simBer,'mx-');
axis([-3 10 10^-5 0.5])
grid on
legend('theory', 'simulation');
xlabel('Eb/No, dB');
ylabel('Bit Error Rate');
title('Bit error probability curve for BPSK modulation');
```

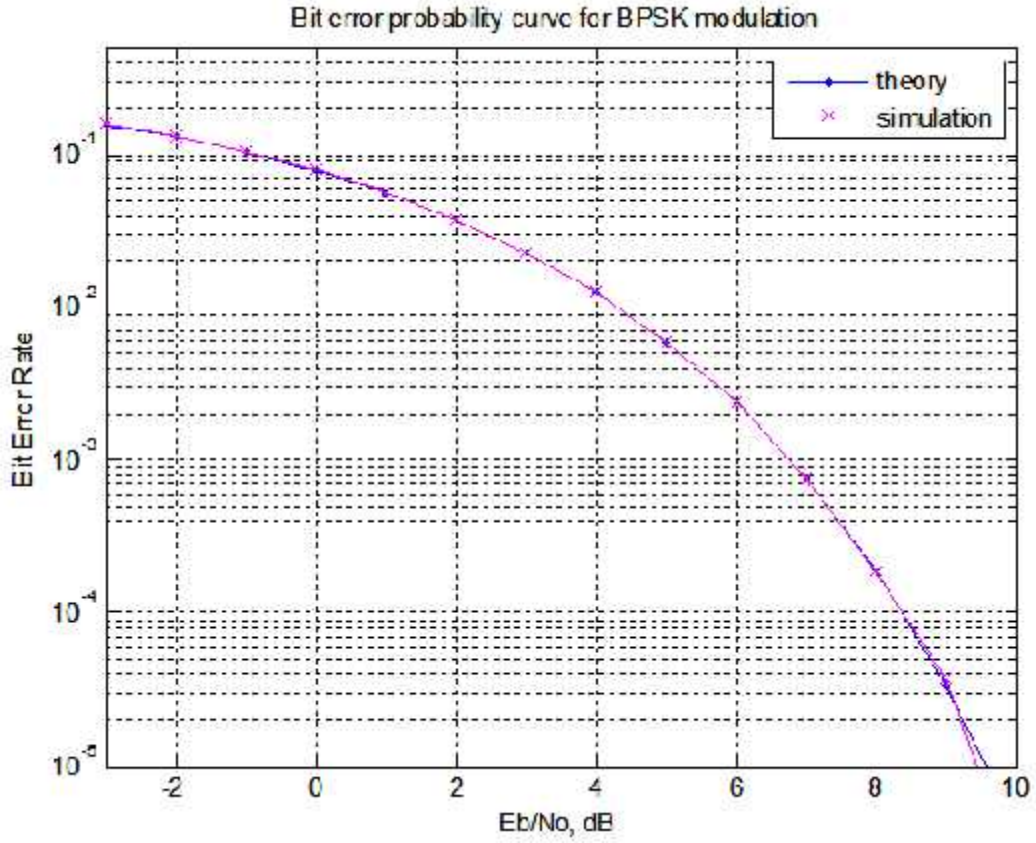


Fig.9.3

Results: - Thus the program for computing the bit error rate with BPSK modulation is written using MATLAB and verified.

Discussion&Conclusions:

Write briefly your comments about the above experiment.

EXPERIMENT # 10

Title: SIMULATION STUDY OF PROBABILITY OF SYMBOL ERROR FOR BFSK MODULATION

Objective:Bit Error Rate (BER) for BFSK modulation

Theory:

In binary Frequency shift keying (BFSK), the bits 0's and 1's are represented by signals $s_1$and s_2 having frequencies f_1 and $f_2$respectively, i.e.

$$s_i(t) = \sqrt{\frac{2E}{T}}\cos(2\pi f_1 t + \phi)$$

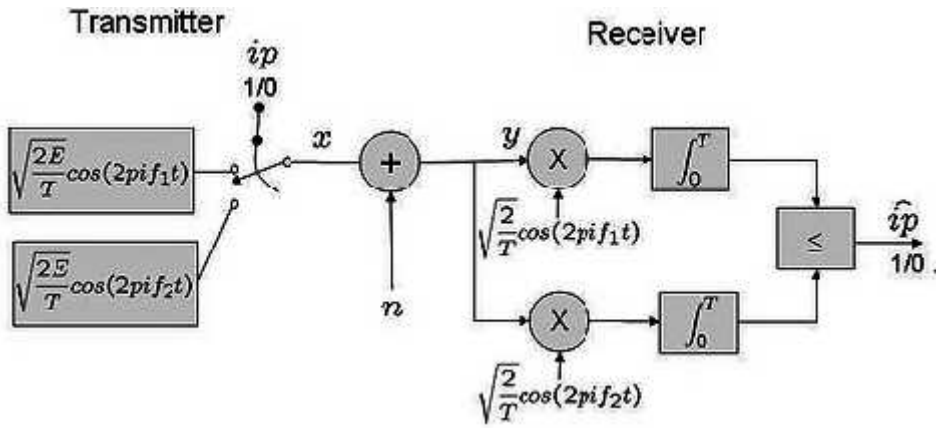
where
E is the energy,
T is the symbol duration and
$\phi$is an arbitrary phase (assume to be zero).

The two frequencies f_1 and f_2 are orthogonal, i.e.

$$\int_0^T \sqrt{\frac{2E}{T}}\cos(2\pi f_1 t + \phi)\sqrt{\frac{2}{T}}\cos(2\pi f_2 t + \phi)dt = \sqrt{E} \text{ and}$$

$$\int_0^T \sqrt{\frac{2E}{T}}\cos(2\pi f_1 t + \phi)\sqrt{\frac{2}{T}}\cos(2\pi f_2 t + \phi)dt = 0$$

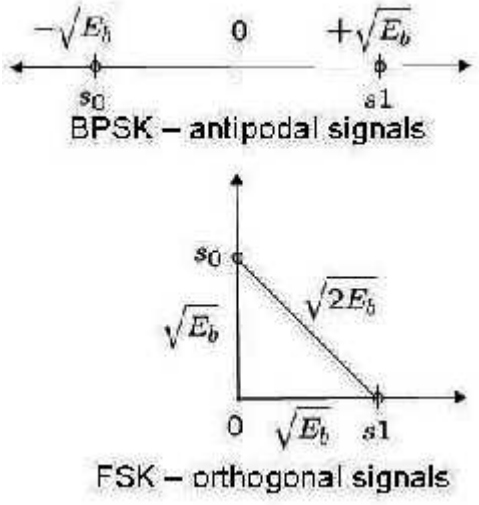
Simple transmit-receive block diagram for binary frequency shift keying (FSK) can be as shown below.



Block diagram of FSK modulation and coherent demodulation: Fig. 10.1

For analyzing the **bit error rate with coherent FSK demodulation**, let us compare the signaling waveform used by binary FSK when compared with binary PSK. The distance between the energy of the signaling waveform for:

(a) Binary Phase Shift Keying (BPSK) is 4 E_b(uses antipodal signaling)
(b) Binary Frequency Shift Keying (BFSK) is 2 E_b(uses orthogonal signaling)



Orthogonal and antipodal signaling: Fig 10.2

Using similar mathematical formulation used for BPSK, but with the distance between the signals reduced by half, the bit error probability for coherent binary frequency shift keying is

$$P_b = \frac{1}{2}\operatorname{erfc}\left(\sqrt{\frac{E_b}{2N_0}}\right)$$

For obtaining the same bit error rate as BPSK, binary frequency shift keying requires around 3dB more E_b / N_0.

Simulation Model:

Simple MATLAB script for computing the bit error rate with FSK modulation. The code performs the following:

a) Generation of random 1's and 0's
b) Converting bits to appropriate frequency
c) Passing through Additive White Gaussian Noise channel
d) Demodulation at the receiver
e) Counting the number of errors.

MATLAB Code:-

```
clear
N = 10^5 % number of bits or symbols
T = 8; % symbol duration
t = [0:1/T:0.99]; % sampling instants
tR = kron(ones(1,N),t); % repeating the sampling instants

Eb_N0_dB = [0:11]; % multiple Eb/N0 values

for ii = 1:length(Eb_N0_dB)
% generating the bits
ip = rand(1,N)>0.5; % generating 0,1 with equal probability
freqM = ip+1; % converting the bits into frequency, bit0 -> frequency of
1, bit1 -> frequency of 2
freqR = kron(freqM,ones(1,T)); % repeating
   x = (sqrt(2)/sqrt(T))*cos(2*pi*freqR.*tR); %generating the FSK
modulated signal

   % noise
   n = 1/sqrt(2)*[randn(1,N*T) + j*randn(1,N*T)]; % white gaussian noise,
0dB variance

% coherent receiver
   y = x + 10^(-Eb_N0_dB(ii)/20)*n; % additive white gaussian noise
   op1 = conv(y, sqrt(2/T)*cos(2*pi*1*t)); % correlating with frequency 1
   op2 = conv(y, sqrt(2/T)*cos(2*pi*2*t)); % correlating with frequency 2

   % demodulation
ipHat = [real(op1(T+1:T:end)) < real(op2(T+1:T:end))]; %
nErr(ii) = size(find([ip - ipHat]),2); % counting the number of errors

end
simBer = nErr/N;
theoryBer = 0.5*erfc(sqrt((10.^(Eb_N0_dB/10))/2)); %theoretical BER

close all
figure
semilogy(Eb_N0_dB,theoryBer,'b-');
hold on
semilogy(Eb_N0_dB,simBer,'mx-');
axis([0 11 10^-4 0.5])
grid on
legend('theory:fsk-coh', 'sim:fsk-coh');
xlabel('Eb/No, dB')
ylabel('Bit Error Rate')
title('Bit error probability curve')
```

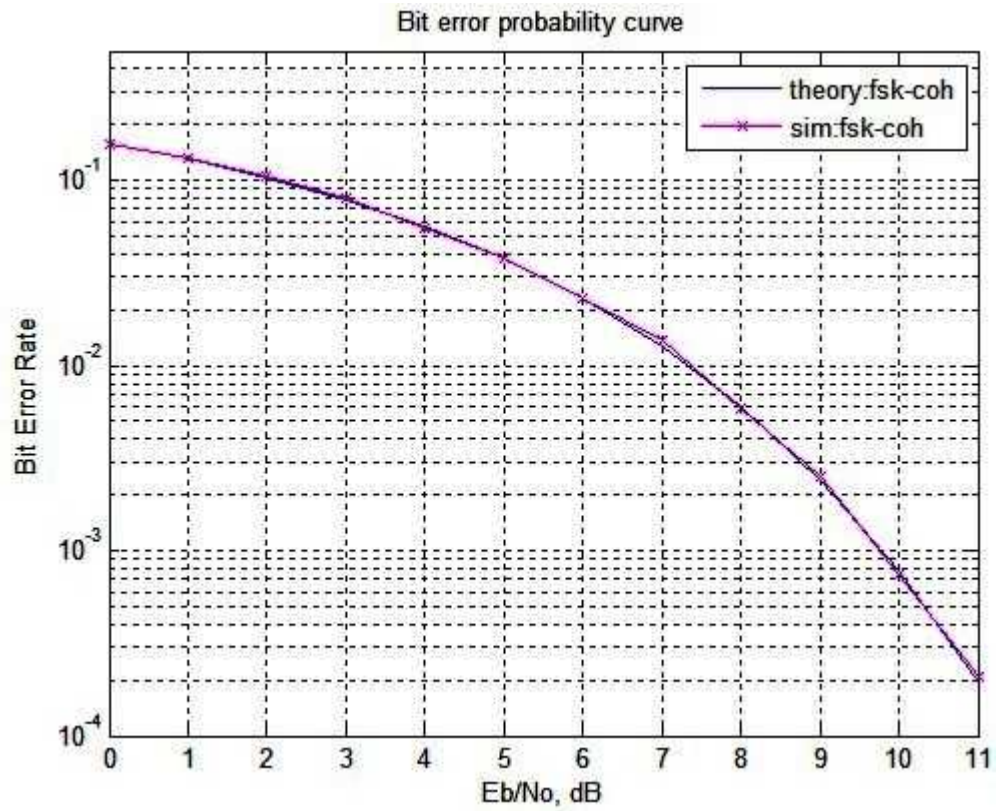


Fig 10.3

Results: - Thus the program for computing the bit error rate with BFSK modulation is written using MATLAB and verified.

Discussion&Conclusions:

Write briefly your comments about the above experiment.

Electronics and Communication Engineering Department

Continuous Lab assessment for 5ECE

Digital Communication Lab [EC 592]

EN: ***Experiment No.***
FA: ***File Assessment***
PRFM:** **Performance-
E = Excellent (10), G = Good (8),
F = Fair (6), P = Poor (4),

SL.	Roll No.	Name	UNIV Roll No.	Week-			Week-			Week-			Week-			Week-		
				EN	FA	*PRFM	EN	FA	*PRFM	EN	FA	*PRFM	EN	FA	*PRFM	EN	FA	*PRFM
1	ECE/24/001	DURBADAL ROUTH	10700324010															
2	ECE/24/002	ANIKET PANDA	10700324009															
3	ECE/24/003	SHUBHANKAR BOS	10700324008															
4	ECE/24/004	RATUL ROY	10700324007															
5	ECE/24/005	DEVDIPTA MONDA	10700324006															
6	ECE/24/006	SRIJIT DAS	10700324005															
7	ECE/24/007	RIYA HEMBRAM	10700324004															
8	ECE/24/008	SUSMITA SENA	10700324003															
9	ECE/24/009	SOUMEN MANNA	10700324014															
10	ECE/24/010	SWARNAVA DAS	10700324001															
11	ECE/24/011	SAYAN SAMANTA	10700324002															
12	ECE/24/012	ANKAN MAITI	10700324013															
13	ECE/24/013	ARUP MAITY	10700324012															
14	ECE/24/015	NIBEDITA DAS	10700324011															
			Name of the Teacher															
			Signature with date															

Exp. No.	Experiment Details	Performed in

4

LABORATORYNAME: ……………………………………………………………………………..……...

NAME:……………………………………………COLLEGEROLLNO.……………………

IndexSheet

SL	TitleoftheExperiment	Exp.No.	Date ofExperiment	Date ofSubmission	Page No.	Grade	Teacher'sSignature
						☐E ☐G ☐F ☐P ☐NS	
						☐E ☐G ☐F ☐P ☐NS	
						☐E ☐G ☐F ☐P ☐NS	
						☐E ☐G ☐F ☐P ☐NS	
						☐E ☐G ☐F ☐P ☐NS	
						☐E ☐G ☐F ☐P ☐NS	
						☐E ☐G ☐F ☐P ☐NS	
						☐E ☐G ☐F ☐P ☐NS	
						☐E ☐G ☐F ☐P ☐NS	

** E: Excellent G: Good F: Fair P: Poor NS: Not Submitted